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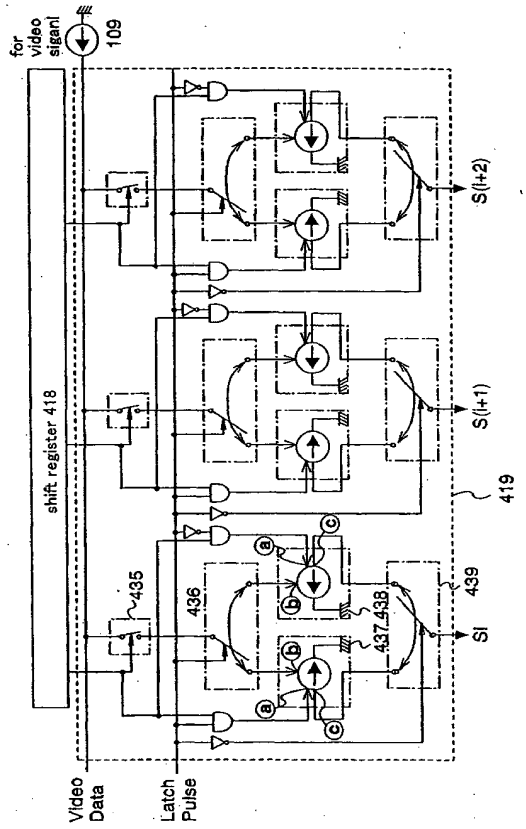
(54) SIGNAL LINE DRIVE CIRCUIT AND LIGHT EMITTING DEVICE

(57) Variations occur in the characteristics of transistors. The present invention is a signal-line drive circuit comprising first and second current source circuits corresponding to respective plurality of signal lines, a shift register, and n (n is a natural number of one or more) video-signal constant current source s, wherein each of the first and second current source circuits has a capacitance means and a supply means. The capacitance means held in one of the first and second source circuits converts a current including a current supplied from each of the n video-signal constant current source s to voltage in response to a sampling pulse supplied from the shift register and a latch pulse supplied from the exterior; and the supply means held in the other supplies a current responsive to the converted voltage. The values of the currents supplied from the n video-signal constant current source s are set to a proportion of 2^0: 2^1:··· :2^n.

Fig. 4



EP 1 486 942 A1

Description

Technical Field

[0001] The present invention relates to a technique of a signal line drive circuit. Further, the present invention relates to a light emitting device including the signal line drive circuit.

Background Art

[0002] Recently, display devices for performing image display are being developed. Liquid crystal display devices that perform image display by using a liquid crystal element are widely used as display devices because of advantages of high image quality, thinness, lightweight, and the like.

[0003] In addition, light emitting devices using self-light emitting elements as light emitting elements are recently being developed. The light emitting device has characteristics of, for example, a high response speed suitable for motion image display, low voltage, and low power consumption, in addition to advantages of existing liquid crystal display devices, and thus, attracts a great deal of attention as the next generation display device.

[0004] As gradation representation methods used in displaying a multi-gradation image on a light emitting device, an analog gradation method and a digital gradation method are given. The former analog gradation method is a method in which the gradation is obtained by analogously controlling the magnitude of a current that flows in a light emitting element. The latter digital gradation method is a method in which the light emitting element is driven only in two states thereof: an ON state (state where the luminance is substantially 100%) and an OFF state (state where the luminance is substantially 0%). In the digital gradation method, since only two gradations can be displayed, a method configured by combining the digital gradation method and a different method to display multi-gradation images has been proposed.

[0005] When classification is made based on the type of a signal that is input to pixels, a voltage input method and a current input method are given as pixel-driving methods. The former voltage input method is a method in which: a video signal (voltage) that is input to a pixel is input to a gate electrode of a driving element; and the driving element is used to control the luminance of a light emitting element. The latter current input method is a method in which the set signal current is flown in a light emitting element to control the luminance of the light emitting element.

[0006] Hereinafter, referring to Fig. 16A, a brief description will be made on an example of a circuit of a pixel in a light emitting device employing the voltage input method and a driving method thereof. The pixel shown in Fig. 16A includes a signal line 501, a scanning line 502, a switching TFT 503, a driving TFT 504, a capacitor device 505, a light emitting element 506, and power sources 507 and 508.

[0007] When the potential of the scanning line 502 varies, and the switching TFT 503 is turned ON, a video signal that has been input to the signal line 501 is input to a gate electrode of the driving TFT 504. According to the potential of the input video signal, a gate-source voltage of the driving TFT 504 is determined, and a current flowing between the source and the drain of the driving TFT 504 is determined. This current is supplied to the light emitting element 506, and the light emitting element 506 emits light. As a semiconductor device for driving the light emitting element, a polysilicon transistor is used. However, the polysilicon transistor is prone to variation in electrical characteristics, such as a threshold value and an ON current, due to defects in a grain boundary. In the pixel shown in Fig. 16A, if characteristics of the driving TFT 504 vary in units of the pixel, even when identical video signals have been input, the magnitudes of the corresponding drain currents of the driving TFTs 504 are different. Thus, the luminance of the light emitting element 506 varies.

[0008] To solve the problems described above, a desired current may be input to the light emitting element, regardless of the characteristics of the TFTs for driving the light emitting element. From this viewpoint, the current input method has been proposed which can control the magnitude of a current that is supplied to a light emitting element regardless of the TFT characteristics.

[0009] Next, referring to Figs. 16B and 17, a brief description will be made with respect to a circuit of a pixel in a light emitting device employing the current input method and a driving method thereof. The pixel shown in Fig. 16B includes a signal line 601, first to third scanning lines 602 to 604, a current line 605, TFTs 606 to 609, a capacitor element 610, and a light emitting element 611. A current source circuit 612 is disposed to each signal line (each column).

[0010] Operations of from video signal-writing to light emission will be described by using Fig. 17. In Fig. 17, reference numerals denoting respective portions conform to those shown in Fig. 16. Figs. 17A to 17C schematically show current paths. Fig. 17D shows the relationship between currents flowing through respective paths during a write of a video signal, and Fig. 17E shows a voltage accumulated in the capacitor device 610 also during the write of a video signal, that is, a gate-source voltage of the TFT 608.

[0011] First, a pulse is input to the first and second scanning lines 602 and 603 to turn the TFTs 606 and 607 ON. A signal current flowing through the signal line 601 at this time will be referred to as I_{data}. As shown in Fig. 17A, since the signal current I_{data} is flowing through the signal line 601, the current separately flows through current paths I_1 and I_2 in the pixel. Fig. 17D shows the relationship between the currents. Needless to say, the relationship is expressed as $I_{data} = I_1 + I_2$.

[0012] The moment the TFT 606 is turned ON, no

charge is yet accumulated in the capacitor device 610, and thus, the TFT 608 is OFF. Accordingly, $I_2 = 0$ and $I_{data} = I_1$ are established. In the moment, the current flows between electrodes of the capacitor device 610, and charge accumulation is performed in the capacitor device 610.

[0013] Charge is gradually accumulated in the capacitor device 610, and a potential difference begins to develop between both the electrodes (Fig. 17E). When the potential difference of both the electrodes has reached V_{th} (point A in Fig. 17E), the TFT 608 is turned ON, and I_2 occurs. As described above, since $I_{data} = I_1 + I_2$ is established, while I_1 gradually decreases, the current keeps flowing, and charge accumulation is continuously performed in the capacitor device 610.

[0014] In the capacitor device 610, charge accumulation continues until the potential difference between both the electrodes, that is, the gate-source voltage of the TFT 608 reaches a desired voltage. That is, charge accumulation continues until the voltage reaches a level at which the TFT 608 can allow the current I_{data} to flow. When charge accumulation terminates (B point in Fig. 17E), the current I_1 stops flowing. Further, since the TFT 608 is fully ON, $I_{data} = I_2$ is established (Fig. 17B). According to the operations described above, the operation of writing the signal to the pixel is completed. Finally, selection of the first and second scanning lines 602 and 603 is completed, and the TFTs 606 and 607 are turned OFF.

[0015] Subsequently, a pulse is input to the third scanning line 604, and the TFT 609 is turned ON. Since V_{GS} that has been just written is held in the capacitor device 610, the TFT 608 is already turned ON, and a current equal to I_{data} flows thereto from the current line 605. Thus, the light emitting element 611 emits light. At this time, when the TFT 608 is set to operate in a saturation region, even if the source-drain voltage of the TFT 608 varies, a light emitting current I_{EL} flowing to the light emitting element 611 flows without variation.

[0016] As described above, the current input method refers to a method in which the drain current of the TFT 609 is set to have the same current value as that of the signal current I_{data} set in the current source circuit 612, and the light emitting element 611 emits light with the luminance corresponding to the drain current. By using the thus structured pixel, the effects of the characteristic variations of TFTs constituting the pixel is reduced, and a desired current can be supplied to the light emitting element.

[0017] Incidentally, in the light emitting device employing the current input method, a signal current corresponding to a video signal needs to be precisely input to a pixel. However, when a signal line drive circuit (corresponding to the current source circuit 612 in Fig. 16) used to input the signal current to the pixel is constituted by polysilicon transistors, variation in characteristics thereof occurs, thereby also causing variation in characteristics of the signal current.

[0018] That is, in the light emitting element employing the current input method, influence by variation in characteristics of TFTs constituting the pixel and the signal line drive circuit need to be suppressed. However, while the effects of the characteristic variations of TFTs constituting the pixel is reduced by using the pixel having the structure of Fig. 16B, reduction of the effects of characteristic variations of TFTs constituting the signal line drive circuit is difficult.

[0019] Hereinafter, using Fig. 18, a brief description will be made of the structure and operation of a current source circuit disposed in the signal line drive circuit that drives the pixel employing the current input method.

[0020] The current source circuit 612 shown in Figs. 18A and 18B corresponds to the current source circuit 612 of Fig. 16B. The current source circuit 612 includes constant current sources 555 to 558. The constant current sources 555 to 558 are controlled by signals that are input via respective terminals 551 to 554. The magnitudes of currents supplied from the constant current sources 555 to 558 are different from one another, and the ratio thereof is set to 1 : 2 : 4 : 8.

[0021] Fig. 18B shows a circuit structure of the current source circuit 612, in which the constant current sources 555 to 558 shown therein correspond to transistors. The ratio of ON currents of the transistors 555 to 558 is set to 1 : 2 : 4 : 8 according to the ratio (1:2:4:8) of the value of L (gate length)/W (gate width). The current source circuit 612 then can control the current magnitudes at $2^4 = 16$ levels. Specifically, currents having 16-gradation analog values can be output for 4-bit digital video signals. Note that the current source circuit 612 is constituted by polysilicon transistors, and is integrally formed with the pixel portion on the same substrate.

[0022] As described above, conventionally, a signal line drive circuit incorporated with a current source circuit has been proposed (for example, refer to Non-patent Documents 1 and 2).

[0023] In addition, digital gradation methods include a method in which a digital gradation method is combined with an area gradation method to represent multi-gradation images (hereinafter, referred to as area gradation method), and a method in which a digital gradation method is combined with a time gradation method to represent multi-gradation images (hereinafter, referred to as time gradation method). The area gradation method is a method in which one pixel is divided into a plurality of sub-pixels, emission or non-emission is selected in each of the sub-pixels, and the gradation is represented according to a difference between a light emitting area and the other area in a single pixel. The time gradation method is a method in which gradation representation is performed by controlling the emission period of a light emitting element. To be more specific, one frame period is divided into a plurality of subframe periods having mutually different lengths, emission or non-emission of a light emitting element is selected in each period, and the gradation is presented according to a

difference in length of light emission time in one frame period. In the digital gradation method, the method in which a digital gradation method is combined with a time gradation method (hereinafter, referred to as time gradation method) is proposed. (For example, refer to Patent Document 1).

[Non-patent Document 1]

[0024] Reiji Hattori & three others, "Technical Report of Institute of Electronics; Information and Communication Engineers (IEICE) ", ED 2001-8, pp. 7-14, "Circuit Simulation of Current Specification Type Polysilicon TFT Active Matrix-Driven Organic LED Display"

[Non-patent Document 2]

Reiji H et al.; "AM-LCD'01", OLED-4, pp. 223-226

[Patent Document 1]

JP 2001-5426 A

Disclosure of the Invention

[0025] The above-described current source circuit 612 is set such that the ON-state currents of the transistors are in a proportion of 1:2:4:8 by the design of the value L (gate length)/W (gate width). However, in the transistors 555 to 558, many factors including variations in the gate length, gate width, and the thickness of a gate insulator film, which are caused by the difference in manufacturing process and a substrate for use, conspire to cause variations in the threshold value and mobility. Therefore, it is difficult to set the proportion of the ON-state currents of the transistors 555 to 558 to 1:2:4:8 accurately as designed. In brief, the values of currents to be supplied to pixels vary by column.

[0026] In order to set the proportion of the ON-state currents of the transistors 555 to 558 to 1:2:4:8 accurately as designed, all the characteristics of the current source circuits in all columns must be the same. In other words, it is necessary for all the characteristics of the transistors of the current source circuits held in the signal-line drive circuit to be the same; however, it is extremely difficult to realize.

[0027] The present invention has been made in consideration of the above problems, and provides a signal-line drive circuit capable of reducing the effects of the characteristic variations of TFTs and supplying a desired signal current to pixels. Furthermore, the present invention provides a light emitting device capable of reducing the effects of the characteristic variations of TFTs that constitute both the pixels and the drive circuit and supplying a desired signal current to light-emitting elements using the pixels with the circuit configuration in which the effects of the characteristic variations of TFTs are reduced.

[0028] The present invention provides a signal-line drive circuit with a new configuration equipped with an electrical circuit (referred to as a current source circuit in this specification) that carries a desired constant current with reduced effects of characteristic variations in TFTs. Furthermore, the present invention provides a light emitting device equipped with the signal-line drive circuit described above.

[0029] The present invention provides a signal-line drive circuit having a current source circuit disposed in each column (each signal line and so on).

[0030] In the signal-line drive circuit of the present invention, a signal current is set in the current source circuit arranged in each signal line using a video-signal constant current source. The current source circuit in which the signal current is set is capable of feeding a current proportional to the video-signal constant current source . Thus, the effects of the characteristic variations of TFTs constituting the signal-line drive circuit can be reduced by using the current source circuit.

[0031] The video-signal constant current source may be integrated with the signal-line drive circuit on the substrate. Alternatively, current may be inputted as a video-signal current from the outside of the substrate using an IC or the like. In this case, a constant current or a current responsive to the video signal is supplied as a video-signal current from the exterior of the substrate to the signal-line drive circuit.

[0032] The outline of the signal-line drive circuit of the present invention will be described with reference to Figs. 1 and 2. Figs. 1 and 2 show a signal-line drive circuit around the ith to (i + 2)th three signal lines.

[0033] Referring to Fig. 1, a signal-line drive circuit 403 has a current source circuit 420 arranged in each signal line (each column). The current source circuit 420 has a terminal a, a terminal b, and a terminal c. From the terminal a, a setting signal is inputted. To the terminal b, a current (signal current) is supplied from a video-signal constant current source 109 connected to the current line. From the terminal c, a signal held in the current source circuit 420 is outputted through a switch 101. In other words, the current source circuit 420 is controlled by the setting signal inputted from the terminal a; to which the supplied signal current is inputted through the terminal b; and which outputs a current proportional to the signal current through the terminal c. The switch 101 is arranged between the current source circuit 420 and pixels connected to the signal line, and the ON/OFF of the switch 101 is controlled by a latch pulse.

[0034] Next, a signal-line drive circuit having a different configuration form that of Fig. 1 will be described with reference to Fig. 2. In Fig. 2, the signal-line drive circuit 403 includes two or more current source circuits 420 for each signal line (each column). The current source circuit 420 includes a plurality of current source circuits. Assuming that two current source circuits are provided, the current source circuit 420 includes a first current source circuit 421 and a second current source circuit 422. Each of the first current source circuit 421 and the second current source circuit 422 includes a terminal a, a terminal b, a terminal c, and a terminal d. Through the terminal a, a setting signal is inputted.

Through the terminal b, a current (signal current) is supplied from the video-signal constant current source 109 connected to the current line. Through the terminal c, a signal held in each of the first current source circuit 421 and the second current source circuit 422 is outputted. In other words, the current source circuit 420 is controlled by the setting signal inputted through the terminal a and a control signal inputted through the terminal d; to which the supplied signal current is inputted through the terminal b; and which outputs a current (signal current) proportional to the signal current through the terminal c. The switch 101 is arranged between the current source circuit 420 and pixels connected to the signal line, and the ON/OFF of the switch 101 is controlled by a latch pulse. Through the terminal d, a control signal is inputted.

[0035] In this specification, the operation of bringing the writing of signal current I_{data} to the current source circuit 420 to an end (setting a signal current, setting so as to allow the output of a current proportional to the signal current by the signal current, and defining so that the current source circuit 420 can output the signal current) is called a setting operation; and the operation of inputting the signal current I_{data} to pixels (operation of the current source circuit 420 to output a signal current) is called an inputting operation. Referring to Fig. 2, since the control signals inputted to the first current source circuit 421 and the second current source circuit 422 are different from each other, one of the first current source circuit 421 and the second current source circuit 422 performs setting operation and the other performs inputting operation. Thus, the two operations can be performed at the same time.

[0036] In the present invention, a light emitting device includes a panel having a pixel section including light-emitting elements and a signal-line drive circuit enclosed between the substrate and a cover member; a module mounting an IC and the like on the panel; and a display. In short, the light emitting device corresponds to the general term for the panel, module, and the display.

[0037] The signal-line drive circuit of the present invention includes latches each having a current source circuit. The signal-line drive circuit of the present invention can be applied to both an analog intensity-level system and a digital intensity-level system.

[0038] According to the present invention, the TFT can be replaced with a general transistor using a single crystal, a transistor using an SOI (silicon on insulator), an organic transistor and so on for application.

[0039] The present invention is a signal-line drive circuit comprises first and second current source circuits corresponding to respective plurality of signal lines; a shift register; and n (n is a natural number of one or more) video-signal constant current source s, characterized in that:

each of the first and second current source circuits has a capacitance means and a supply means; wherein

the capacitance means held in one of the first and second source circuits converts a current including a current supplied from each of the n video-signal constant current source s to voltage in accordance with a sampling pulse supplied from the shift register and a latch pulse supplied from the exterior; and

the supply means held in the other supplies a current responsive to the converted voltage; and

the values of the currents to be supplied from the n video-signal constant current source s are set to a proportion of $2^0:2^1:\cdots:2^n$.

[0040] The present invention is a signal-line drive circuit comprising (2 x n) current source circuits corresponding to respective plurality of signal lines; a shift register, and n (n is a natural number of one or more) video-signal constant current source s, characterized in that:

the (2 × n) current source circuits includes a capacitance means for converting a current supplied from either one of the n video-signal constant current source s to voltage in accordance with a sampling pulse supplied from the shift register and a latch pulse supplied from the exterior; and a supply means for supplying a current corresponding to the converted voltage;

a current is supplied to each of the plurality of signal lines from the n current source circuits selected from the (2 × n) current source circuits; and

the values of the currents to be supplied from the n video-signal constant current source s are set to a proportion of $2^0:2^1:\cdots:2^n$.

[0041] The signal-line drive circuit with the foregoing configuration according to the present invention includes a shift register and a latch having two or more current source circuits. The current source circuit having a supply means and a capacitance means can supply a predetermined value of current without being affected by the characteristic variations of the constituting transistors. The signal-line drive circuit has a logical operator. A sampling pulse supplied from the shift register and a latch pulse supplied from the exterior are inputted to the two input terminals of the logical operator. In the present invention, the two or more current source circuits disposed in the latch are controlled using a signal outputted from the output terminal of the logical operator. In this case, the operation of converting the supplied current to a voltage can accurately be performed in the current source circuit over a long period of time.

[0042] In the present invention, there is provided a signal-line drive circuit having the foregoing current source circuits. Furthermore, in the present invention, there is provided a light emitting device capable of reducing the effects of the characteristic variations in TFTs

that constitute both the pixels and the drive circuit, and supplying a desired signal current I_{data} to light-emitting elements by using pixels with the circuit configuration in which the effects of the characteristic variations in TFTs are reduced.

Brief Description of the Drawings

[0043]

Fig. 1 is a view of a signal line drive circuit.
Fig. 2 is a view of a signal line drive circuit.
Fig. 3 is views of a signal line drive circuit (1-bit, 2-bit).
Fig. 4 is a view of a signal line drive circuit (1-bit).
Fig. 5 is a view of a signal line drive circuit (2-bit).
Fig. 6 is a circuit diagram of current source circuits.
Fig. 7 is a circuit diagram of current source circuits.
Fig. 8 is a circuit diagram of current source circuits.
Fig. 9 is a circuit diagram of a video-signal current source.
Fig. 10 is a circuit diagram of a video-signal current source.
Fig. 11 is a circuit diagram of a video-signal current source.
Fig. 12 is a view of the appearance of a light emitting device according to the present invention.
Fig. 13 is a circuit diagram of pixels of a light emitting device.
Fig. 14 is an explanatory view of a driving method of a light emitting device according to the present invention.
Fig. 15 is a view of a light emitting device of the present invention.
Fig. 16 is a circuit diagram of a pixel in a light emitting device.
Fig. 17 is an explanatory view of operations of a pixel in the light emitting device.
Fig. 18 is a view of a current source circuit.
Fig. 19 is an explanatory view of operations of a current source circuit.
Fig. 20 is an explanatory view of operations of a current source circuit.
Fig. 21 is an explanatory view of operations of a current source circuit.
Fig. 22 is a view of an electronic device to which a light emitting device according to the present invention is applied.
Fig. 23 is a circuit diagram of a video-signal current source .
Fig. 24 is a circuit diagram of a video-signal current source .
Fig. 25 is a circuit diagram of a video-signal current source .
Fig. 26 is a view of a signal line drive circuit (2-bit).
Fig. 27 is a circuit diagram of a current source.
Fig. 28 is a circuit diagram of a current source.
Fig. 29 is a circuit diagram of a current source.
Fig. 30 is a circuit diagram of a current source.
Fig. 31 is a circuit diagram of a current source.
Fig. 32 is a circuit diagram of a current source.
Fig. 33 is a view showing a signal line drive circuit.
Fig. 34 is a view showing a signal line drive circuit.
Fig. 35 is a view showing a signal line drive circuit.
Fig. 36 is a view showing a signal line drive circuit.
Fig. 37 is a view showing a signal line drive circuit.
Fig. 38 is a view showing a signal line drive circuit.
Fig. 39 is a view showing a signal line drive circuit.
Fig. 40 is a view showing a signal line drive circuit.
Fig. 41 is a view showing a signal line drive circuit.
Fig. 42 is a view showing a signal line drive circuit.
Fig. 43 is a view showing a signal line drive circuit.
Fig. 44 is a circuit diagram of a video-signal current source.
Fig. 45 is a circuit diagram of a video-signal current source.
Fig. 46 is a circuit diagram of a video-signal current source.
Fig. 47 is a circuit diagram of a video-signal current source.
Fig. 48 is a view of a signal line drive circuit.
Fig. 49 is a layout view of a current source circuit.
Fig. 50 is a circuit diagram of a current source circuit.

Best Mode for carrying but the Invention

[First Embodiment]

[0044] In this embodiment, an example of a circuit structure and its operation of a current source circuit 420 which is supplied in a signal line drive circuit of the present invention will be described.

[0045] In the invention, a setting signal input from a terminal a represents a signal input from an output terminal of a logical operator. In other words, the setting signal in Fig. 1 corresponds to the signal input from the output terminal of the logical operator. In the present invention, the setting operation of the current source circuit 420 is performed in accordance with the signal input from the output terminal of the logical operator.

[0046] One of two input terminals of the logical operator is input with a sampling pulse from a register, and the other is input with a latch pulse. In the logical operator, a logic operation of two signals which have been input is performed, and a signal from the output terminal is output. Then in the current source circuit, the setting operation or the input operation is performed according to the signal input from the output terminal of the logical operator.

[0047] Note that a shift register has a structure including, for example, flip-flop circuits (FFs) in a plurality of columns. A clock signal (S-CLK), a start pulse (S-SP), and an inverted clock signal (S-CLKb) are input to the shift register, and signals serially output according to the timing of the input signals are called sampling pulses.

[0048] In Fig. 6A, a circuit including switches 104, 105a, and 106, a transistor 102 (n-channel type), and a capacitor device 103 for retaining a gate-source voltage VGS of the transistor 102 corresponds to the current source circuit 420.

[0049] In the current source circuit 420, the switch 104 and the switch 105a are turned ON by a signal input via the terminal a. A current is supplied via a terminal b from a video-signal current source 109 (hereafter referred to as constant current source 109) connected to a current line (video line), and a charge is retained in the capacitor device 103. The charge is retained in the capacitor device 103 until a signal current I_{data} supplied from the constant current source 109 becomes identical with a drain current of the transistor 102.

[0050] Then, the switch 104 and the switch 105a are turned OFF by a signal input via the terminal a. As a result, since the predetermined charge is retained in the capacitor device 103, the transistor 102 is imparted with a capability of flowing a current having a magnitude corresponding to that of the signal current I_{data}. If the switch 101 (signal current control switch) and the switch 106 are turned into a conductive state, a current via a terminal c flows to a pixel connected to the signal line. At this time, since the gate voltage of the transistor 102 is maintained at a predetermined gate voltage in the capacitor device 103. Thus, the effects of the characteristic variations of TFTs constituting the signal line drive circuit is reduced, and the magnitude of the current input to the pixel can be controlled.

[0051] The connection structure of the switch 104 and the switch 105a is not limited to the structures shown in Fig. 6A. For example, the structure may be such that one of terminals of the switch 104 is connected to the terminal b, and the other terminal is connected between itself and the gate electrode of the transistor 102; and one of terminals of the switch 105a is connected to the terminal b via the switch 104, and the other terminal is connected to the switch 106. Then, the switch 104 and the switch 105a are controlled by a signal input from the terminal a.

[0052] Alternatively, the switch 104 may be disposed between the terminal b and the gate electrode of the transistor 104, and the switch 105a may be disposed between the terminal b and the switch 116. Specifically, referring to Fig. 27A, lines, switches, and the like may be disposed such that the connection is structured as shown in Fig. 27(A1) in the setting operation, and the connection is structured as shown in Fig. 27(A2) in the input operation. The number of wirings, the number of switches, and the structure are not particularly limited.

[0053] In the current source circuit 420 of Fig. 6A, the signal setting operation (setting operation) and the signal inputting operation (input operation) to the pixel or the current source circuit, that is, the current outputting operation from the current source circuit cannot be performed simultaneously.

[0054] Referring to Fig. 6B, a circuit including a switch 124, a switch 125, a transistor 122 (n-channel type), a capacitor device 123 for retaining a gate-source voltage VGS of the transistor 122, and a transistor 126 (n-channel type) corresponds to the current source circuit 420.

[0055] The transistor 126 functions as either a switch or a part of a current source transistor.

[0056] In the current source circuit 420 shown in Fig. 6B, the switch 124 and the switch 125 are turned ON by a signal input via the terminal a. Then, a current is supplied via the terminal b from the constant current source 109 connected to the current line, and a charge is retained in the capacitor device 123. The charge is retained therein until the signal current I_{data} flown from the constant current source 109 becomes identical with a drain current of the transistor 122. Note that, when the switch 124 is turned ON, since a gate-source voltage VGS of the transistor 126 is set to 0 V, the transistor 126 is turned OFF.

[0057] Subsequently, the switch 124 and the switch 125 are turned OFF by a signal input via the terminal a. As a result, since a predetermined charge is retained in the capacitor device 123, the transistor 122 is imparted with a capability of flowing a current having a magnitude corresponding to that of the signal current I_{data}. If the switch 101 (signal current control switch) is turned into a conductive state, the current flows to the pixel connected to the signal line via the terminal c. At this time, since the gate voltage of the transistor 122 is maintained by the capacitor device 123 at a predetermined gate voltage, a drain current corresponding to the signal current I_{data} flows to the drain region of the transistor 122. Thus, the effects of the characteristic variations of TFTs constituting the signal line drive circuit is reduced, and the magnitude of the current input to the pixel can be controlled.

[0058] When the switches 124 and 125 have been turned OFF, gate and source potentials of the transistor 126 are varied not to be the same. As a result, since the charge retained in the capacitor device 123 is distributed also to the transistor 126, and the transistor 126 is automatically turned ON. Here, the transistors 122 and 126 are connected in series, and the gates thereof are connected. Accordingly, each of the transistors 122 and 126 serves as a multi-gate transistor. That is, a gate length L of the transistor varies between the setting operation and the input operation. Therefore, the value of the current supplied from the terminal b at the time of the setting operation can be made larger than the value of the current supplied from the terminal c at the time of the input operation. Thus, various loads (such as wiring resistances and cross capacitances) disposed between the terminal b and the constant current source 109 can be charged even faster. Consequently, the setting operation can be completed quickly.

[0059] The number of switches, the number of wirings, and their connection structures are not particularly limited. Specifically, referring to Fig. 27B, wirings and switches may be disposed such that the connection is

structured as shown in Fig. 27(B1) in the setting operation, and the connection is structured as shown in Fig. 27(B2) in the input operation. In particular, in Fig. 27 (C2), it is sufficient that the charge accumulated in a capacitor device 107 does not leak. The number of switches and wirings are not particularly limited.

[0060] Note that, in the current source circuit 420 shown in Fig. 6B, the signal setting operation (setting operation) and the signal inputting operation (input operation) to the pixel, that is, the current outputting operation from the current source circuit cannot be performed simultaneously.

[0061] Referring to Fig. 6C, a circuit including a switch 108, a switch 110, transistors 105b, 106 (n-channel type), and a capacitor device 107 for retaining gate-source voltages VGS of the transistors 150b and 106 corresponds to the current source circuit 420.

[0062] In the current source circuit 420 shown in Fig. 6C, the switch 108 and the switch 110 are turned ON by a signal input via a terminal a. Then, a current is supplied via a terminal b from the constant current source 109 connected to the current line, and a charge is retained in the capacitor device 107. The charge is retained therein until the signal current I_{data} flown from the constant current source 109 becomes identical with a drain current of the transistor 105b. At this time, since the gate electrodes of the transistor 105b and of the transistor 106 are connected to each other, the gate voltages of the transistor 105b and the transistor 106 are retained by the capacitor device 107.

[0063] Then, the switch 108 and the switch 110 are turned OFF by the signal input via the terminal a. As a result, since a predetermined charge is retained in the capacitor device 107, the transistor 106 is imparted with a capability of flowing a current having a magnitude corresponding to that of the signal current I_{data}. If the switch 101 (signal current control switch) is turned to a conductive state, a current flows to the pixel connected to the signal line via a terminal c. At this time, since the gate voltage of the transistor 106 is maintained by the capacitor device 107 at the predetermined gate voltage, a drain current corresponding to the current (the signal current I_{data}) flows to the drain region of the transistor 106. Thus, the effects of the characteristic variations of TFTs constituting the signal line drive circuit is reduced, and the magnitude of the current input to the pixel can be controlled.

[0064] At this time, characteristics of the transistor 105b and the transistor 106 need to be the same to cause the drain current corresponding to the signal current I_{data} to flow precisely to the drain region of the transistor 106. To be more specific, values such as mobility and thresholds of the transistor 105b and the transistor 106 need to be the same In addition, in Fig. 6C, the value of W (gate width)/L (gate length) of each of the transistor 105b and the transistor 106 may be arbitrarily set, and a current proportional to the signal current I_{data} supplied from the constant current source 109 and the like may be supplied to the pixel.

[0065] Further, the value of W/L of the transistor 105b or the transistor 106 that is connected to the constant current source 109 is set high, whereby the write speed can be increased by supplying a large current from the constant current source 109.

[0066] With the current source circuit 420 shown in Fig. 6C, the signal setting operation (setting operation) can be performed simultaneously with the signal inputting operation (input operation) to the pixel.

[0067] Each of the current source circuits 420 of Figs. 6D and 6E has the same circuit element connection structures as that of the current source circuit 420 of Fig. 6C, except for the connection structure of the switch 110. In addition, since the operation of the current source circuit 420 of each of Figs. 6D and 6E conforms to the operation of the current source circuit 420 of Fig. 6C, a description thereof will be omitted in the present embodiment.

[0068] Note that, the number of switches, the number of wirings, and their connection structures are not particularly limited. Specifically, referring to Fig. 27C, wirings and switches may be disposed such that the connection is structured as shown in Fig. 27(C1) in the setting operation, and the connection is structured as shown in Fig. 27(C2) in the input operation. In particular, in Fig. 27(C2), it is sufficient that the charge accumulated in the capacitor device 107 does not leak.

[0069] Referring to Fig. 28A, a circuit including switches 195b, 195c, 195d, and 195f, a transistor 195a, and a capacitor device 195e corresponds to the current source circuit. In the current source circuit shown in Fig. 28A, the switches 195b, 195c, 195d, and 195f are turned ON by a signal input via a terminal a. Then, a current is supplied via a terminal b from the constant current source 109 connected to the current line. A predetermined charge is retained in the capacitor device 195e until the signal current supplied from the constant current source 109 becomes identical with a drain current of the transistor 195a.

[0070] Then, the switches 195b, 195c, 195d, and 195f are turned OFF by a signal input via the terminal a. At this time, since the predetermined charge is retained in the capacitor device 195e, the transistor 195a is imparted with a capability of flowing a current having a magnitude corresponding to that of the signal current. This is because the gate voltage ofthe transistor 195a is set by the capacitor device 195a to a predetermined gate voltage, and a drain current corresponding to a current (reference current) flows to the drain region of the transistor 195a. In this state, a current is supplied to the outside via a terminal c. Note that, in the current source circuit shown in Fig. 28A, the operation for setting the current source circuit to have a capability of flowing a signal current cannot be performed simultaneously with the input operation for inputting the signal current to the pixel. In addition, when a switch controlled by the signal input via the terminal a is ON, and also, when a current

is controlled not to flow from the terminal c, the terminal c needs to be connected to another line of the other potential. Here, the line potential is represented by Va. Va may be a potential sufficient to flow a current flowing from the terminal b as it is, and may be a power supply voltage Vdd as an example.

[0071] Note that, the number of switches, the number of wirings, and their connection structures are not particularly limited. Specifically, referring to Figs. 28B and 28C, wirings and switches may be disposed such that the connection is structured as shown in either Fig. 28 (B1) or 28(C1) in the setting operation, and the connection is structured as shown in either Fig. 28(B2) or 28 (C2) in the input operation. The number of wirings and switches are not particularly limited.

[0072] Further, in the current source circuits of Figs. 6A and 6C to 6E, the current-flow directions (directions from the pixel to the signal line drive circuit) are the same. The polarity (conductivity type) of each of the transistor 102, the transistor 105b, and the transistor 106 can be of p-channel type.

[0073] Fig. 7A shows a circuit structure in which the current-flow direction (direction from the pixel to the signal line drive circuit) is the same, and the transistor 102 shown in Fig. 6A is set to be of p-channel type. In Fig. 7A, with the capacitor device disposed between the gate and the source, even when the source potential varies, the gate-source voltage can be maintained. Further, Figs. 7B to 7D show circuit diagrams in which the current-flow directions (directions from the pixel to the signal line drive circuit) are the same, and the transistor 105b and the transistor 106 shown in Figs. 6C to 6E are set to be of p-channel type.

[0074] Further, Fig. 29A shows a case where the transistor 195a is set to be of p-channel type in the structure of Fig. 28. Fig. 29B shows a case where the transistors 122 and 126 are set to be of p-channel type in the structure of Fig. 6B.

[0075] Referring to Fig. 31, a circuit including switches 104 and 116, a transistor 102, a capacitor device 103, and the like corresponds to the current source circuit.

[0076] Fig. 31A corresponds to the circuit of Fig. 6A that is partly modified. In the current source circuit of Fig. 31A, the transistor gate width W varies between the setting operation of the current source and the input operation. Specifically, in the setting operation, the connection is structured as shown in Fig. 31B, in which the gate width W is large. In the input operation, the connection is structured as shown in Fig. 31C, in which the gate width W is small. Therefore, the value of the current supplied from the terminal b at the time of the setting operation can be made larger than the value of the current supplied from the terminal c at the time of the input operation. Thus, various loads (such as wiring resistances and cross capacitances) disposed between the terminal b and the constant current source for the video signal can be charged even faster. Consequently, the setting operation can be completed quickly.

[0077] Note that, Fig. 31 shows the circuit of Fig. 6A that is partly modified. In addition, the circuit can be easily applied to, for example, other circuits shown in Fig. 6 and to the circuits shown in Fig. 7, Fig. 28, Fig. 30, and Fig. 29.

[0078] Note that, in the above mentioned current source circuits, a current flows from the pixel to the signal line drive circuit. However, the current not only flows from the pixel to the signal line drive circuit, but also may flow from the signal line drive circuit to the pixel. It depends on the structure of the pixel that the current flows in a direction from the pixel to the signal line drive circuit or in a direction from the signal line drive circuit to the pixel. In the case where the current flows from the signal line drive circuit to the pixel, Vss (low potential power source) may be set to Vdd (high potential power source), and the transistors 102, 105b, 106, 122, and 126 may be set to be of p-channel type in Fig. 6. Also in the circuit diagram shown in Fig. 7, Vss may be set to Vdd, and the transistors 102, 105b, and 106 may be of n-channel type.

[0079] Note that wirings and switches may be disposed such that the connection is structured as shown in Figs. 30 (A1) to (D1) in the setting operation, and the connection is structured as shown in Figs. 30 (A2) to (D2) in the input operation. The number of switches, the number of wirings and their connection structures are not particularly limited.

[0080] Note that, in all the current source circuits described above, the disposed capacitor device may not be disposed by being substituted by, for example, a gate capacitance of a transistor.

[0081] Hereinafter, a description will be made in detail regarding the operations of the current source circuits of Figs. 6A, 7A, 6C to 6E, and 7B to 7D among those described above by using Figs. 6 and 7. To begin with, the operations of the current source circuits of Figs. 6A and 7A will be described with reference to Fig. 19.

[0082] Figs. 19A to 19C schematically show paths of a current flowing among circuit elements. Fig. 19D shows the relationship between the current flowing through each path and the time when the signal current I_{data} is written to the current source circuit. Fig. 19E shows the relationship between the voltage accumulated in a capacitor device 16, that is, the gate-source voltage of a transistor 15, and the time when the signal current I_{data} is written to the current source circuit. In the circuit diagrams of Figs. 19A to 19C, numeral 11 denotes a video-signal current source, each of switches 12 to 14 is a semiconductor device having a switching function, numeral 15 denotes a transistor (n-channel type), numeral 16 denotes a capacitor device, and numeral 17 denotes a pixel. In this embodiment, the switch 14, the transistor 15, and the capacitor device 16 form an electric circuit corresponding to a current source circuit 20. Drawing lines and reference symbols are shown in Fig. 19A. Since drawing lines and reference symbols shown in Figs. 19B and 19C are similar to those shown

in Fig. 19A, they are omitted here.

[0083] A source region of the n-channel transistor 15 is connected to Vss, and a drain region thereof is connected to the video-signal current source 11. One of electrodes of the capacitor device 16 is connected to Vss (the source of the transistor 15), and the other electrode is connected to the switch 14 (the gate of the transistor 15). The capacitor device 16 plays a role of holding the gate-source voltage of the transistor 15.

[0084] Note that, in practice, the current source circuit 20 is supplied in the signal line drive circuit. A current corresponding to the signal current I_{data} flows via, for example, a circuit element included in the signal line or the pixel from the current source circuit 20 supplied in the signal line drive circuit. However, since Fig. 19 is a diagram for briefly explaining the outline of the relationship among the video-signal current source 11, the current source circuit 20, and the pixel 17, a detailed illustration of the structure is omitted.

[0085] First, an operation (setting operation) of the current source circuit 20 for retaining the signal current I_{data} will be described by using Figs. 19A and 19B. Referring to Fig. 19A, the switch 12 and the switch 14 are turned ON, and the switch 13 is turned OFF. In this state, the signal current I_{data} is output from the video-signal current source 11, and flows to the current source circuit 20 from the video-signal current source 11. At this time, since the signal current I_{data} is flowing from the video-signal current source 11, the current flows separately through current paths I_1 and I_2 in the current source circuit 20, as shown in Fig. 19A. Fig. 19D shows the relationship at this time. Needless to say, the relationship is expressed as $I_{data} = I_1 + I_2$.

[0086] The moment the current starts to flow from the video-signal current source 11, since no charge is accumulated in the capacitor device 16, the transistor 15 is OFF. Accordingly, $I_2 = 0$ and $I_{data} = I_1$ are established. A charge is gradually accumulated into the capacitor device 16, and a potential difference begins to occur between both electrodes of the capacitor device 16 (Fig. 19E). When the potential difference of both the electrodes has reached V_{th} (point A in Fig. 19E), the transistor 15 is turned ON, and $I_2>0$ is established. As described above, since $I_{data} = I_1 + I_2$, while I_1 gradually decreases, the current keeps flowing. The charge accumulation is continuously performed in the capacitor device 16.

[0087] The potential difference between both the electrodes of the capacitor device 16 serves as the gate-source voltage of the transistor 15. Thus, the charge accumulation in the capacitor device 16 continues until the gate-source voltage of the transistor 15 reaches a desired voltage, that is, a voltage (VGS) that allows the transistor is to be flown with the current I_{data}. When the charge accumulation terminates (B point in Fig. 19E), the current I_1 stops flowing. Further, since the TFT 15 is ON, $I_{data} = I_2$ is established (Fig. 19B).

[0088] Next, an operation (input operation) for inputting the signal current I_{data} to the pixel will be described by using Fig. 19C. When the signal current I_{data} is input to the pixel, the switch 13 is turned ON, and the switch 12 and the switch 14 are turned OFF. Since VGS written in the above-described operation is held in the capacitor device 16, the transistor 15 is ON. A current identical with the signal current I_{data} flows to Vss via the switch 13 and transistor 15, and the input of the signal current I_{data} to the pixel is then completed. At this time, when the transistor 15 is set to operate in a saturation region, even if the source-drain voltage of the transistor 15 varies, a current flowing into the pixel can flows constantly.

[0089] In the current source circuit 20 shown in Fig. 19, as shown in Figs. 19A to 19C, the operation is divided into an operation (setting operation; corresponding to Figs. 19A and 19B) for completing a write of the signal current I_{data} to the current source circuit 20, and an operation (input operation; corresponding to Fig. 19C) for inputting the signal current I_{data} to the pixel). Then, in the pixel, a current is supplied to the light emitting element in accordance with the input signal current I_{data}.

[0090] The current source circuit 20 of Fig. 19 is not capable of performing the setting operation and the input operation simultaneously. In the case where the setting operation and the input operation need to be performed simultaneously, at least two current source circuits are preferably supplied to each of a plurality of signal lines each of which is connected with a plurality of pixels and which are provided in a pixel portion. However, if the setting operation can be performed within a period during which the signal current I_{data} is not input to the pixel, only one current source circuit may be provided for each signal line (each column).

[0091] Although the transistor 15 of the current source circuit 20 shown in each of Figs. 19A to 19C is of n-channel type, the transistor 15 of the current source circuit 20 may be of p-channel type, of course. Here, a circuit diagram for the case where the transistor 15 is of p-channel type is shown in Fig. 19. Referring to Fig. 19F, numeral 31 denotes a video-signal current source , each switches 32 to 34 is a semiconductor device (transistor) having a switching function, numeral 35 denotes a transistor (p-channel type), numeral 36 denotes a capacitor device, and numeral 37 denotes a pixel. In this embodiment, the switch 34, the transistor 35, and the capacitor device 36 form an electric circuit corresponding to a current source circuit 24.

[0092] The transistor 35 is of p-channel type. One of a source region and a drain region of the transistor 35 is connected to Vdd, and the other is connected to the constant current source 31. One of electrodes of the capacitor device 36 is connected to Vdd, and the other electrode is connected to the switch 36. The capacitor device 36 plays a role of holding the gate-source voltage of the transistor 35.

[0093] An operation of the current source circuit 24 of Fig. 19F is similar to that of the current source circuit 20 described above, except for the current-flow direction,

and thus, a description thereof will be omitted here. In the case of designing the current source circuit in which the polarity of the transistor 15 is changed without changing the current-flow direction, the circuit diagram of Fig. 7A may be referenced.

[0094] Note that in Fig. 32, the current-flow direction is the same as in Fig. 19F, in which the transistor 35 is of n-channel type. The capacitor device 36 is connected between the gate and the source of the transistor 35. The source potential of the transistor 35 varies between the setting operation and the input operation. However, even when the source potential varies, since the gate-source voltage is retained, a normal operation is implemented.

[0095] Next, operations of the current source circuits shown in Figs. 6C to 6E and Figs. 7B to 7D will be described by using Figs. 20 and 21. Figs. 20A to 20C schematically show paths through which a current flows among circuit elements. Fig. 20D shows the relationship between the current flowing through each path and the time when the signal current I_{data} is written to the current source circuit. Fig. 20E shows the relationship between the voltage accumulated in a capacitor device 46, that is, the gate-source voltages of transistor 43, 44, and the time when the signal current I_{data} is written to the current source circuit. Further, in the circuit diagrams of Figs. 20A to 20C, numeral 41 denotes a video-signal current source , a switch 42 is a semiconductor device having a switching function, numerals 43 and 44 denote transistors (n-channel type), numeral 46 denotes a capacitor device, and numeral 47 denotes a pixel. In this embodiment, the switch 42, the transistors 43 and 44, and the capacitor device 46 compose an electric circuit corresponding to a current source circuit 25. Note that drawing lines and reference symbols are shown in Fig. 20A, and since drawing lines and reference symbols shown in Figs. 20B and 20C conform to those shown in Fig. 20A, they are omitted.

[0096] A source region of the n-channel transistor 43 is connected to Vss, and a drain region thereof is connected to the video signal current source 41. A source region of the n-channel transistor 44 is connected to Vss, and a drain region thereof is connected to a terminal 48 of the light emitting element 47. One of electrodes of the capacitor device 46 is connected to Vss (the sources of the transistors 43 and 44), and the other electrode thereof is connected to the gate electrodes of the transistors 43 and 44. The capacitor device 46 plays a role of holding gate-source voltages of the transistors 43 and 44.

[0097] Note that, in practice, the current source circuit 25 is provided in the signal line drive circuit. A current corresponding to the signal current I_{data} flows via, for example, a circuit element included in the signal line or the pixel, from the current source circuit 25 provided in the signal line drive circuit. However, since Fig. 20 is a diagram for briefly explaining the outline of the relationship among the video-signal current source 41, the current source circuit 25, and the pixel 47, a detailed illustration of the structure is omitted.

[0098] In the current source circuit 25 of Fig. 20, the sizes of the transistors 43 and 44 are important. Hereinafter, using different reference symbols, a case where the sizes of the transistors 43 and 44 are identical and a case the sizes are mutually different will be described. Referring to Figs. 20A to 20C, the case where the sizes of the transistors 43 and 44 are mutually identical will be described by using the signal current I_{data}. The case where the sizes of the transistors 43 and 44 are mutually different will be described by using a signal current I_{data1} and a signal current I_{data2}. Note that the sizes of the transistors 43 and 44 are determined by using the value of W (gate width)/L (gate length) of each transistor.

[0099] First, the case where the sizes of the transistors 43 and 44 are mutually identical will be described. To begin with, operations for retaining the signal current I_{data} in the current source circuit 20 will be described by using Figs. 20A and 20B. Referring to Fig. 20A, when the switch 42 is turned ON, the signal current I_{data} is set in the video signal current source 41, and flows from the video-signal current source 41 to the current source circuit 25. At this time, since the signal current I_{data} is flowing from the video-signal current source 41, the current flows separately through current paths I_1 and I_2 in the current source circuit 20, as shown in Fig. 20A. Fig. 20D shows the relationship at this time. Needless to say, the relationship is expressed as $I_{data} = I_1 + I_2$.

[0100] The moment the current starts to flow from the video signal current source 41, since no charge is yet accumulated in the capacitor device 46, the transistors 43 and 44 are OFF. Accordingly, $I_2 = 0$ and $I_{data} = I_1$ are established.

[0101] Then, a charge is gradually accumulated into the capacitor device 46, and a potential difference begins to occur between both electrodes of the capacitor device 46 (Fig. 20E). When the potential difference of both the electrodes has reached V_{th} (point A in Fig. 20)), the transistors 43 and 44 are turned ON, and $I_2>0$ is established. As described above, since $I_{data} = I_1 + I_2$, while I_1 gradually decreases, the current keeps flowing. The charge accumulation is continuously performed in the capacitor device 46.

[0102] The potential difference between both the electrodes of the capacitor device 46 serves as the gate-source voltage of each of the transistors 43 and 44. Thus, the charge accumulation in the capacitor device 46 continues until each the gate-source voltages of the transistors 43 and 44 reaches a desired voltage, that is, a voltage (VGS) that allows the transistor 44 to be flown with the current I_{data}. When the charge accumulation terminates (B point in Fig. 20E), the current I_1 stops flowing. Further, since the transistors 43 and 44 are ON, $I_{data} = I_2$ is established (Fig. 20B).

[0103] Next, an operation for inputting the signal current I_{data} to the pixel will be described by using Fig. 20C. First, the switch 42 is turned OFF. Since VGS written at

the above-described operation is retained in the capacitor device 46, the transistors 43 and 44 are ON. A current identical with the signal current I_{data} flows from the pixel 47. Thus, the signal current I_{data} is input to the pixel. At this time, when the transistor 44 is set to operate in a saturation region, even if the source-drain voltage of the transistor 44 varies, the current flowing in the pixel can be flown without variation.

[0104] In the case of a current mirror circuit shown in Fig. 6C, even when the switch 42 is not turned OFF, a current can be flown to the pixel 47 by using the current supplied from the video signal current source 41. That is, the setting operation for setting a signal for the current source circuit 20 can be implemented simultaneously with the operation (input operation) for inputting a signal to the pixel.

[0105] Next, a case where the sizes of the transistors 43 and 44 are mutually different will be described. An operation of the current source circuit 25 is similar to the above-described operation; therefore, a description thereof will be omitted here. When the sizes of the transistors 43 and 44 are mutually different, the signal current I_{data1} set in the video signal current source 41 is inevitably different from the signal current I_{data2} that flows to the pixel 47. The difference therebetween depends on the difference between the values of W (gate width)/L (gate length) of the transistors 43 and 44.

[0106] In general, the W/L value of the transistor 43 is preferably set larger than that of the transistor 44. This is because the signal current I_{data1} can be increased when the W/L value of the transistor 43 is set large. In this case, when the current source circuit is set with the signal current I_{data1}, Loads (cross capacitances, wiring resistances) can be charged. Thus, the setting operation can be completed quickly.

[0107] The transistors 43 and 44 of the current source circuit 25 in each of Figs. 20A to 20C are of n-channel type, but the transistors 43 and 44 of the current source circuit 25 may be of p-channel type. Here, Fig. 21 shows a circuit diagram in which the transistors 43 and 44 are of p-channel type.

[0108] Referring to Fig. 21, numeral 41 denotes a constant current source, a switch 42 is a semiconductor device having a switching function, numerals 43 and 44 denote transistors (p-channel type), numeral 46 denotes a capacitor device, and numeral 47 denotes a pixel. In this embodiment, the switch 42, the transistors 43 and 44, and the capacitor device 46 form an electric circuit corresponding to a current source circuit 26.

[0109] A source region of the p-channel transistor 43 is connected to Vdd, and a drain region thereof is connected to the constant current source 41. A source region of the p-channel transistor 44 is connected to Vdd, and a drain region thereof is connected to a terminal 48 of the light emitting element 47. One of electrodes of the capacitor device 46 is connected to (source), and the other electrode is connected to the gate electrodes of the transistors 43 and 44. The capacitor device 46 plays a role of holding gate-source voltages of the transistors 43 and 44.

[0110] The operation of the current source circuit 24 of Fig. 21 is similar to that shown in each of Figs. Figs. 20A to 20C except for the current-flow direction, and thus, a description thereof will be omitted here. In the case of designing the current source circuit in which the polarities of the transistors 43 and 44 are changed without changing the current-flaw direction, Fig. 7B and Fig. 32 may be referenced.

[0111] In summary, in the current source circuit of Fig. 19, the current having the same magnitude as that of the signal current I_{data} set in the constant current source flows to the pixel. In other words, the signal current I_{data} set in the constant current source is identical in value with the current flowing to the pixel. The current is not effected by characteristic variations of transistors supplied in the current source circuit.

[0112] In each of the current source circuits of Fig. 19 and Fig. 6B, the signal current I_{data} cannot be output to the pixel from the current source circuit in a period during which the setting operation is performed. Thus, two current source circuits are preferably provided for each signal line, in which an operation (setting operation) for setting a signal is performed to one of the current source circuits, and an operation (input operation) for inputting I_{data} to the pixel is performed using the other current source circuit.

[0113] However, in the case where the setting operation and the input operation are not performed at the same time, only one current source circuit may be provided for each column. The current source circuit of each of Figs. 28A and 29A is similar to the current source circuit of Fig. 19, except for the connection and current-flow paths. The current source circuit of Fig. 31A is similar, except for the difference in magnitude between the current supplied from the constant current source and the current flowing from the current source circuit. The current source circuits of Figs. 6B and 29B are similar, except for the difference in magnitude between the current supplied from the constant current source and the current flowing from the current source circuit. Specifically, in Fig. 31A, only the gate width W of the transistor is different between the setting operation and the input operation; in Figs. 6B and 29B, only the gate length L is different between the setting operation and the input operation; and others are similar to those of the structure of the current source circuit in Fig. 19.

[0114] In each of the current source circuits of Figs. 20 and 21, the signal current I_{data} set in the constant current source and the value of the current flowing to the pixel are dependent on the sizes of the two transistors provided in the current source circuit. In other words, the signal current I_{data} set in the constant current source and the current flowing to the pixel can be arbitrarily changed by arbitrarily designing the sizes (W (gate width)/L (gate length)) of the two transistors provided in the current source circuit. However, output of a

precise signal current I_{data} to the pixel is difficult in the case where variation is caused in the characteristics of the two transistors, such as threshold values and mobility.

[0115] Further, in each of the current source circuits of Figs. 20 and 21, the signal can be input to the pixel during the setting operation. That is, the setting operation for setting the signal can be performed simultaneously with the operation (input operation) for inputting the signal to the pixel. Thus, unlike the current source circuit of Fig. 19, two current source circuits do not need to be provided in a single signal line.

[0116] The present invention with the above structure can reduce the effects of characteristic variations in the TFT and supply a desired current to the outside.

[Second embodiment]

[0117] The above has described that, for a current source circuit like the one shown in Fig. 6 (and, Figs. 19, 31A, 6B, 29B, or the like), preferably, two current source circuits are provided for each signal line (each column), in which one of the current source circuits is used to perform the signal setting operation (set operation), and the other current source circuit is used to perform the I_{data} input operation (input operation) to the pixel. This is because the setting operation and the input operation cannot be performed simultaneously. In this embodiment, an exemplary circuit structure of the current source circuit 420 shown in Fig. 2, which has a signal drive circuit of the present invention, will be described with reference to Fig. 8.

[0118] In the present invention, a setting signal input from a terminal a represents a signal input from an output terminal of a logical operator. In other words, the setting signal in Fig. 1 corresponds to the signal input from the output terminal of the logical operator. In the present invention, the setting operation of the current source circuit 420 is performed in accordance with the signal input from the output terminal of the logical operator.

[0119] One of two input terminals of the logical operator is input with a sampling pulse from a register, and the other is input with a latch pulse. In the logical operator, a logic operation of two signals which have been input is performed, and a signal from the output terminal is output. Then in the current source circuit, the setting operation or the input operation is performed according to the signal input from the output terminal of the logical operator.

[0120] The current source circuit 420 is controlled by a setting signal input via the terminal a, and is input with a signal current supplied from the terminal b, thereby the current source circuit 420 outputs a current proportional to the signal current (a video-signal current) from the terminal c.

[0121] Referring to Fig. 8A, a circuit including switches 134 to 139, a transistor 132 (n-channel type), and a capacitor device 133 for retaining a gate-source voltage VGS of the transistor 132 corresponds to the first current source circuit 421 or the second current source circuit 422.

[0122] In the first current source circuit 421 or the second current source circuit 422, the switch 134 and the switch 136 are turned ON by the signal input via the terminal a. Further, the switch 135 and the switch 137 are turned ON by the signal input from the control line via the terminal d. Then, a current (a video-signal current) is supplied via the terminal b from the video-signal current source 109 connected to the current line, and a charge is retained in the capacitor device 133. The charge is retained in the capacitor device 133 until the signal current I_{data} flown from the video-signal current source 109 becomes identical with a drain current of the transistor 132.

[0123] Subsequently, the switches 134 to 137 are turned OFF by the signals input via the terminals a and d. As a result, since a predetermined charge is retained in the capacitor device 133, the transistor 132 is imparted with a capability of flowing a current having a magnitude corresponding to that of the signal current I_{data}. If the switches 101, 138 and 139 are turned into a conductive state, a current flows to a pixel connected to the signal line via the terminal c. At this time, since the gate voltage of the transistor 132 is maintained by the capacitor device 133 at the predetermined gate voltage, a drain current corresponding to the signal current I_{data} flows to the drain region of the transistor 132. Thus, the effects of the characteristic variations of TFTs constituting the signal line drive circuit is reduced, and the magnitude of the current input to the pixel can be controlled.

[0124] Referring to Fig. 8B, a circuit including switches 144 to 147, a transistor 142 (n-channel type), a capacitor device 143 for retaining a gate-source voltage VGS of the transistor 142, and a transistor 148 (n-channel type) corresponds to the first current source circuit 421 or the second current source circuit 422.

[0125] In the first current source circuit 421 or the second current source circuit 422, the switch 144 and the switch 146 are turned ON by the signal input via the terminal a. Further, the switch 145 and the switch 147 are turned ON by the signal input from the control line via the terminal d. Then, a current is supplied via the terminal b from the constant current source 109 connected to the current line, and a charge is retained in the capacitor device 143. The charge is retained in the capacitor device 143 until a signal current I_{data} that is flown from the constant current source 109 becomes identical with a drain current of the transistor 142. When the switch 144 and the switch 145 are turned ON, since a gate-source voltage VGS of the transistor 148 is set to 0 V, the transistor 148 is automatically turned OFF.

[0126] Subsequently, the switches 144 to 147 are turned OFF by the signals input via the terminals a and d. As a result, since the signal current I_{data} is retained in the capacitor device 143, the transistor 142 has a capability of flowing a current having a magnitude corre-

sponding to that of the signal current I_{data}. If the switch 101 is turned to a conductive state, a current is supplied to a pixel connected to the signal line via the terminal c. At this time, since the gate voltage of the transistor 142 is maintained by the capacitor device 143 at a predetermined gate voltage, a drain current corresponding to the signal current I_{data} flows to a drain region of the transistor 142. Thus, the effects of the characteristic variations of TFTs constituting the signal line drive circuit is reduced, and the magnitude of the current input to the pixel can be controlled.

[0127] When the switches 144 and 145 have been turned OFF, gate and source potentials of the transistor 126 are varied not to be the same. As a result, since the charge retained in the capacitor device 143 is distributed also to the transistor 148, and the transistor 148 is automatically turned ON. Here, the transistors 142 and 148 are connected in series, and the gates thereof are connected. Accordingly, each of the transistors 142 and 148 serves as a multi-gate transistor. That is, a gate length L of the transistor varies between the setting operation and the input operation. Therefore, the value of the current supplied from the terminal b at the time of the setting operation can be made larger than that from the terminal c at the time of the input operation. Thus, various loads (such as wiring resistances and cross capacitances) disposed between the terminal b and the video-signal current source can be charged even faster. Consequently, the setting operation can be completed quickly.

[0128] Note that Fig. 8A corresponds to a structure in which the terminal d is added to the structure of Fig. 6A. Fig. 8B corresponds to a structure in which the terminal d is added to the structure of Fig. 6B. Thus, the structures of Figs. 6A and 6B are added with switches in series, thereby being modified to those of Figs. 8A and 8B each of which is added with the terminal d. The structure of the current source circuit shown in, for example, Fig. 6, 7, 28, 29, or 31 can be arbitrarily used by arranging two switches in series in the first current source circuit 421 or the second current source circuit 422 of Fig. 2.

[0129] The structure in which the current source circuit 420 including for each signal line the two current source circuits, namely, the first and second current source circuits 421 and 422, is shown in Fig. 2. However, the present invention is not limited to this. For example, three current source circuits 420 may be provided for each signal line. Then, a signal current may be set by different r constant current sources 109 for the respective current source circuits 420. For example, it may be such that a 1-bit video-signal current source is used to set a signal current for one of the current source circuit 420, a 2-bit video-signal current source is used to set a signal current for one of the current source circuits 420, and a 3-bit video-signal current source is used to set a signal current for one of the current source circuits 420. Thus, 3-bit display can be performed.

[0130] This embodiment may be arbitrarily combined with first embodiment. That is, as shown in Figs. 4, 5, 26 and 27, current source circuits of Fig. 6 can be disposed such that two current source circuits are disposed in each column as shown in Fig. 2 from that one current source circuit is disposed in each column. Then, for example, in Fig. 2, assuming that a current supplied from the current source circuit 421 is 4.9A, a current supplied from the current source circuit 422 is 5.1A, by supplying a current from either the current source circuit 421 or the current source circuit 422 in each frame, variation of the current source circuits can be averaged.

[0131] This embodiment may be arbitrarily combined with first embodiment.

[Third embodiment]

[0132] In this embodiment, the structure of a light emitting device including the signal line drive circuit of the present invention will be described using Fig. 15.

[0133] The light emitting device includes a pixel portion 402 including a plurality of pixels arranged in matrix on a substrate 401, and includes a signal line drive circuit 403 and a first scanning line drive circuit 404 and a second scanning line drive circuit 405 in the periphery of the pixel portion 402. While the signal line drive circuit 403 and the two scanning line drive circuits 404 and 405 are provided in Fig. 15A, the present invention is not limited to this. The number of drive circuits may be arbitrarily designed depending on the pixel structure. Signals are supplied from the outside to the signal line drive circuit 403, the first scanning line drive circuit 404 and the second scanning line drive circuit 405 via FPCs 406.

[0134] The structures and operations of the first scanning line drive circuit 404 and the second scanning line drive circuit 405 will be described using Fig. 15B. Each the first scanning line drive circuit 404 and the second scanning line drive circuit 405 includes a shift register 407 and a buffer 408. If the operation is described briefly, the shift register 407 sequentially outputs sampling pulses in accordance with a clock signal (G-CLK), a start pulse (S-SP), and an inverted clock signal (G-CLKb). Thereafter, the sampling pulses amplified in the buffer 408 are input to scanning lines, and the scanning lines are set to be in a selected state for each line. Signals are sequentially written to pixels controlled by the selected signal lines.

[0135] Note that the structure may be such that a level shifter circuit is disposed between the shift register 407 and the buffer 408. Disposition of the level shifter circuit enables the voltage amplitude to be increased.

[0136] The structure of the signal line drive circuit 403 will be hereafter described. This embodiment may be arbitrarily combined with Embodiments 1 and 2.

[Fourth Embodiment]

[0137] In this embodiment, the configuration and the operation of the signal-line drive circuit 403 shown in Fig. 15A will be described. In this embodiment, the sig-

nal-line drive circuit 403 used for performing analog intensity-level assigning or 1-bit digital intensity-level assigning will be described with reference to Fig. 3A and Fig. 4.

[0138] Fig. 3A is a schematic diagram of the signal-line drive circuit 403 in analog intensity-level assigning or 1-bit digital intensity-level assigning. The signal-line drive circuit 403 includes a shift register 418 and a latch circuit 419.

[0139] A brief description of the operation will be given. The shift register 418 is configured using a plurality of columns of flip-flop circuits (FFs), to which a clock signal (S-CLK), a start pulse (S-SP), and a clock inversion signal (S-CLKb) are inputted Sampling pulses are outputted in sequence in accordance with the timing of such signals.

[0140] The sampling pulses outputted from the shift register 418 are inputted to the latch circuit 419. To the latch circuit 419, a video signal (an analog video signal or a digital video signal) are inputted, which are held in each column in accordance with the timing of inputting the sampling pulses.

[0141] A constant current source 109 for a video signal is connected to a video line. A signal current (corresponding to the video signal) set in the video-signal constant current source 109 is held in the latch circuit 419.

[0142] A latch pulse is inputted to the latch circuit 419, and the video signal held in the latch circuit 419 is inputted to pixels connected to the signal line. The latch circuit 419 is sometimes responsible for converting a digital signal to an analog signal.

[0143] Next, the configuration of the latch circuit 419 will be described with reference to Fig. 4. Fig. 4 shows the outline of the signal-line drive circuit 403 around the ith to (i+2)th three signal lines.

[0144] The latch circuit 419 includes a switch 435, a switch 436, a current source circuit 437, a current source circuit 438, and a switch 439 for each column. The switch 435 is controlled by the sampling pulse inputted from the shift register 418. The switch 436 and the switch 439 are controlled by the latch pulses.

[0145] To the switch 436 and the switch 439, inverted signals from each other are inputted. As a result, one of the current source circuit 437 and the current source circuit 438 performs setting operation and the other performs inputting operation.

[0146] In other words, when the current source circuit 437 performs setting operation, the current source circuit 438 outputs a signal current to pixels, thus performing inputting operation at the same time. In this manner, the setting operation and the inputting operation of the current source s can be performed at the same time, allowing the setting operation to be accurately performed over a long period of time.

[0147] This allows line-sequential driving.

[0148] The signal current supplied from the video line (video data line) has a magnitude depending on the video signal. Thus, the amount of current supplied to the pixels is proportional to the signal current, allowing the provision of an image (a tone image).

[0149] The current source circuit 437 and the current source circuit 438 are controlled by the signal inputted through the terminal a. The current source circuit 437 and the current source circuit 438 also hold a current (signal current I_{data}) set using the video-signal constant current source 109 connected to the video line (current line) via the terminal b. The switch 439 is arranged between the current source circuit 437 and the current source circuit 438 and the pixels connected to the signal line, wherein the On/OFF of the switch 439 is controlled by the latch pulse.

[0150] For performing 1-bit digital intensity-level assigning, when the video signal is a light signal, the signal current I_{data} is outputted from the current source circuit 437 or the current source circuit 438 to the pixels. On the other hand, when the video signal is a dark signal, the current source circuit 437 or the current source circuit 438 has no ability of feeding current, thus feeding no current to the pixels. For performing analog intensity-level assigning, a signal current I_{data} is outputted from a current source circuit 433 to the pixels in response to the video signal. More specifically, in the current source circuit 437 and the current source circuit 438, the capacity (V_{GS}) of feeding a constant current is controlled by the video signal; thus, the brightness is controlled depending on the magnitude of the current outputted to the pixels.

[0151] In the present invention, a setting signal inputted from the terminal a indicates a signal inputted from the output terminal of the logical operator. In other words, the setting signal in Fig. 1 corresponds to a signal inputted from the output terminal of the logical operator. In the present invention, the current source circuit 420 is set in correspondence with the signal inputted from the output terminal of the logical operator.

[0152] The sampling pulse from the shift register is inputted to one of the two input terminals of the logical operator and the latch pulse is inputted to the other. The logical operator performs logical operation of the two inputted signal and outputs a signal from the output terminal. In the current source circuits, setting operation or inputting operation is performed in response to the signal inputted from the output terminal of the logical operator.

[0153] The current source circuit 437 and the current source circuit 438 may freely employ the configuration of the current source circuits shown in Figs. 6 and 7, Fig. 29, Fig. 28, and Fig. 31. The current source circuits may not employ only one system but a plurality of systems.

[0154] In Fig. 4, while the latch circuits are configured for one column from the video-signal constant current source 109, it is not limited to that. As shown in Fig. 33, a plurality of columns may be configured at the same time; in other words, polyphase configuration is possible. While Fig. 33 shows an arrangement of two video-signal constant current source s 109, another video-sig-

nal constant current source may be perform setting operation for the two video-signal constant current source s.

[0155] The following are examples of a combination system of the current source circuit 437 and the current source circuit 438 and the advantages thereof.

[0156] First, an example of employing a circuit of Fig. 6A for the current source circuit 437 and the current source circuit 438 will be described. Using a current source circuit as in Fig. 6A allows the decrease of the number of transistors to be arranged, thus further reducing the effects of variations in the characteristics of the transistors. In other words, since a transistor for setting operation and a transistor for inputting operation are the identical transistor, they are not affected by the variations between the transistors at alL However, since the current in setting operation cannot be increased, setting operation cannot be performed more quickly. The current in setting operation corresponds to the current supplied to the latch circuit from the video-signal constant current source 109.

[0157] The circuit diagram in this case is shown in Fig. 34.

[0158] In Fig. 34, a current flows from the pixels toward the current source circuit through a signal line. However, the direction of the current varies depending on the pixel configuration. Therefore, Fig. 35 shows a circuit diagram when a current flows from the circuit source circuit toward the pixels.

[0159] In this manner, a circuit in the case where the direction of the current is different can be configured by changing the polarities of the transistors. Alternatively, by using a circuit of Fig. 7A in place of Fig. 6A, a circuit in the case where the direction of the current is different can also be configured without changing the polarities of the transistors.

[0160] Next, a case where a current mirror circuit as shown in Fig. 6C is employed as the current source circuit 437 and the current source circuit 438 will be described with reference to Fig. 36.

[0161] In the two transistors of the current mirror circuit as in Fig. 6C, when the value of W (gate width)/L (gate length) of the transistor connected to the pixels is made lower than that of the transistor connected to the video-signal constant current source 109, the current value supplied from the video-signal constant current source 109 can be made high.

[0162] In other words, the value W/L of the transistor for setting operation is set higher than the value W/L of the transistor for inputting operation. Then, the current for setting operation, that is, the current flowing from the video-signal constant current source 109 to the latch circuit can be made high. High current allows electrical charge to quickly be carried to a wiring cross capacitance accompanying wirings, thereby entering a steady state quickly. Thus, setting operation can be performed more quickly.

[0163] The current mirror circuit as in Fig. 6C includes at least two transistors having a gate electrode in common or electrically connected thereto. When the two transistors vary in characteristics, the currents outputted from the source terminals or drain terminals of the transistors also vary. However, if the two transistors have identical characteristics, the currents outputted therefrom do not vary. Conversely, the characteristics of the two transistors need to be identical in order not to vary the outputted currents. In other words, in the current mirror circuit as in Fig. 6C, it is sufficient for the two transistors having a gate electrode in common or electrically connected thereto to have identical characteristics. There is no need for transistors having no common gate electrode to have the identical characteristics. This is because setting operation is performed for each current source circuit. In other words, it is sufficient for the transistor for the setting operation and the transistor used for inputting operation to have the identical characteristics. Even when the transistors having no common gate electrode have not identical characteristics, setting operation is performed for each current source circuit; therefore, variations in characteristics are corrected.

[0164] In general, in the current mirror circuit as in Fig. 6C, the two transistors having a gate electrode in common or electrically connected thereto are arranged in close proximity to each other in order to reduce the variations in the characteristics of the two transistors.

[0165] Referring to Fig. 36, let the magnitude of current applied to the pixels be P. In the two transistors of the current mirror circuit as in Fig. 6C in the current source circuits (the current source circuits 437 and 438), if the value W/L of the transistor connected to the pixels is Wa, the value W/L of the transistor connected to the video signal line is set to ($2 \times$ Wa). Then, the current value becomes twice in the current source circuits (the current source circuits 437 and 438). Then, the video-signal constant current source 109 supplies a current of ($2 \times$ P). Consequently, since the current supplied from the video-signal constant current source 109 can be made high, the setting operation for the current source circuits (the current source circuits 437 and 438) can be performed quickly and accurately.

[0166] In summary, by employing the current mirror circuit as in Fig. 6C for a current source circuit and setting the value W/L to an appropriate value, the current supplied from the video-signal constant current source 109 can be made high. As a result, the setting operation for the current source circuit can be performed accurately.

[0167] In other words, high current allows electrical charge to be carried quickly to a wiring cross capacitance parasitic on wirings, thereby entering a steady state. In the steady state, setting operation can be performed sufficiently. In performing the setting operation in a certain period of time, high current allows the circuit to enter a steady state quickly; thus, the setting operation can be performed sufficiently. If current is low, the duration of setting operation is completed before enter-

ing the steady state. In such a case, for lack of sufficient time, accurate setting operation cannot be performed. Therefore, high current allows quick and accurate setting operation for the current source circuit.

[0168] However, the current mirror circuit as in Fig. 6C includes at least two transistors having a gate electrode in common or electrically connected thereto, wherein the variations in the characteristics of the two transistors cause the variations of the current outputted therefrom.

[0169] However, the magnitude of the current can be varied by setting the ratio W/L of the channel width W and the channel length L of the transistor to different values between the two transistors. Generally, the current in setting operation is set high, thus allowing quick setting operation.

[0170] The current in setting operation corresponds to the current supplied from the video-signal constant current source 109.

[0171] On the other hand, when the circuit as in Fig. 6A is used, the current flowing in setting operation and the current flowing in inputting operation are substantially equal. Therefore, the current for setting operation cannot be set high. However, the transistor for supplying current in setting operation and the transistor for supplying current in inputting operation are the identical. Therefore, they are not affected by the variations between the transistors at alL Accordingly, it is preferable to use an appropriate combination in the latch circuit, such as to use the current mirror circuit as in Fig. 6C for part where high current is desired in setting operation and to use the circuit as in Fig. 6A for part where more accurate current is desired to output.

[0172] Fig. 48 shows a circuit diagram when the current mirror circuit as in Fig. 6C is used in a low-order-bit (first-bit) current source circuit and the circuit as in Fig. 6A is used in a high-order-bit (second-bit) current source circuit.

[0173] Transistors operated only as switches may have either polarity.

[0174] Fig. 4 showed a case in which the circuit of Fig. 2 was applied to the circuit of Fig. 3A. Subsequently, a case in which the circuit of Fig. 1 is applied to the circuit of Fig. 3A will be described with reference to Fig. 37.

[0175] Referring to Fig. 37A, a video signal (signal current) supplied over a video line is supplied to a current source circuit. The setting operation for the current source circuit is performed in accordance with the timing of a sampling pulse supplied from the shift register 418. For example, with the configuration of Fig. 37A, the inputting operation (current output to pixels) is started after the setting operation of the current source circuit, thus allowing point sequential drive to be performed by sequentially setting the current source circuit on a column-by-column basis and then performing inputting operation.

[0176] Fig. 37A shows a case of analog intensity-level assigning or a 1-bit digital intensity level; and Fig. 38 shows a case of 2-bit digital intensity level.

[0177] Fig. 39 shows a circuit when the circuit of Fig. 38 employs the circuit of Fig. 6A. Fig. 40 shows a circuit when the circuit of Fig. 38 employs the circuit of Fig. 6C. Furthermore, Fig. 41 shows a circuit when a 1-bit current source circuit employs the circuit of Fig. 6C, and a 2-bit current source circuit employs the circuit of Fig. 6A. In the circuit of Fig. 41, the magnitude of the video signal current is increased by changing the value W/L of the 1-bit current source circuit. Consequently, the setting operation can be performed in substantially the same period of time as that of the 2-bit current source circuit.

[0178] However, in sequential selection from the first to last column, it takes a long period of time to input signals to pixels in columns closer to the first. On the other hand in columns closer to the last, pixels in the next row are selected immediately after the video signal has been inputted, resulting in a decreased period of time for inputting signals to pixels. In such a case, as shown in Fig. 37B, scanning-lines disposed in the pixel section 402 are divided at the center to increase the duration of inputting signals to the pixels. In that case, a scanning-line drive circuit is arranged on each of the left and right of the pixel section 402, wherein the pixels are driven using the scanning-line drive circuit. With such an arrangement, even for the pixels arranged in the same row, the duration of inputting signals can be changed between the right pixels and the left pixels. Fig. 37C shows output waveforms of the right and left scanning-line drive circuits in the first and second rows and a start pulse (S-SP) of the shift register 411. Since the duration of inputting signals to even the left pixels can be increased by the operation as the waveform in Fig. 37C, thus facilitating point sequential driving.

[0179] In the signal-line drive circuit of the present invention, the layout diagram of the current source circuit arranged in a latch is illustrated in Fig. 49; and a circuit diagram corresponding thereto is shown in Fig. 50.

[0180] This embodiment can freely be combined with the first to third embodiments.

[Fifth Embodiment]

[0181] In this embodiment, a detailed configuration and the operation of the signal-line drive circuit 403 shown in Fig. 15A will be described. In this embodiment, the signal-line drive circuit 403 used for performing 2-bit digital intensity-levels assigning will be described with reference to Fig. 3B, Fig. 5, and Fig. 26.

[0182] Fig. 3B is a schematic diagram of the signal-line drive circuit 403 in performing 2-bit digital intensity-level assigning. The signal-line drive circuit 403 includes the shift register 418 and the latch circuit 419.

[0183] A brief description of the operation will be given. The shift register 418 is configured using a plurality of columns of flip-flop circuits (FFs), to which a clock signal (S-CLK), a start pulse (S-SP), and a clock inversion signal (S-CLKb) are inputted. Sampling pulses are outputted in sequence in accordance with the timing of

such signals.

[0184] The sampling pulses outputted from the shift register 418 are inputted to the latch circuit 419. To the latch circuit 419, a 2-bit digital video signal (digital data 1 and digital data 2) is inputted, which is held in each column in accordance with the timing of inputting the sampling pulses.

[0185] A 1-bit digital video signal is inputted over a current line connected to the 1-bit video-signal constant current source 109. The 2-bit digital video signal is inputted over a current line connected to the 2-bit video-signal constant current source 109. The signal current (corresponding to the video signal) set in the 1-bit and 2-bit video-signal constant current source s 109 is held in the latch circuit 419.

[0186] A latch pulse is inputted to the latch circuit 419, and the 2-bit digital video signal (digital data 1 and digital data 2) held in the latch circuit 419 is inputted to pixels connected to the signal line. The latch circuit 419 is sometimes responsible for converting the digital signal to an analog signal.

[0187] Next, the configuration of the latch circuit 419 will be described with reference to Fig. 5. Fig. 5 shows the outline of the signal-line drive circuit 403 for performing 2-bit digital intensity-level assigning around the ith to (i+1)th two signal lines. Similarly, Fig. 26 shows the outline of a signal-line drive circuit for performing 2-bit digital intensity-level assigning around the ith to (i+1)th two signal lines.

[0188] Fig. 5 shows a case in which the video-signal constant current source s 109 corresponding to the respective bits are arranged.

[0189] Referring to Fig. 5, the latch circuit 419 includes a switch 435a, a switch 436a, a current source circuit 437a a current source circuit 438a, and a switch 439a for each column, and also includes a switch 435b, a switch 436b, a current source circuit 437b, a current source circuit 438b, and a switch 439b for each column.

[0190] The switch 435a and the switch 435b are controlled by the sampling pulses inputted from the shift register 418. The switch 436a, the switch 439a, the switch 436b, and the switch 439b are controlled by the latch pulses.

[0191] To the switch 436a and the switch 439a, inverted signals from each other are inputted. As a result, one of the current source circuit 437a and the current source circuit 438a performs setting operation and the other performs inputting operation. To the switch 436b and the switch 439b, inverted signals from each other are inputted. As a result, one of the current source circuit 437b and the current source circuit 438b performs setting operation and the other performs inputting operation.

[0192] In other words, when the current source circuit 437 performs setting operation, the current source circuit 438 outputs a signal current to pixels at the same time, thus performing inputting operation. In this manner, since the setting operation and the inputting operation of the current source circuits can be performed at the same time, setting operation can accurately be performed over a long period of time.

[0193] The signal current supplied from the video line (video data line) has a magnitude depending on the video signal. Thus, the magnitude of current supplied to the pixels is proportional to the signal current, allowing the provision of an image.

[0194] This allows line-sequential driving.

[0195] Referring to Fig. 5, the current lines and the video-signal constant current source s are arranged in correspondence with the respective bits. The total amount of the current values supplied from the current source s of respective bits is supplied to the signal lines. In brief, the current constant source circuits have the function of digital-analog conversion.

[0196] Each of the current source circuits (the current source circuits 437a, 438a, 437b, and 438b) has a terminal a, a terminal b, and a terminal c. Each of the current source circuits (the current source circuits 437a, 438a, 437b, and 438b) is controlled by a signal constant inputted through the terminal a, and holds a current (signal current I_{data}) that is set using the video-signal current source 109 connected to the video line via the terminal b. The current set in the 1-bit constant current source 109 is held in the current source circuit 437a and the current source circuit 438a. The current set in the 2-bit constant current source 109 is held in the current source circuit 437b and the current source circuit 438b. The switch 439a and the switch 439b are arranged between each current source circuit (current source circuits 437a, 438a, 437b, and 438b) and the pixels connected to the signal lines, wherein the On/OFF of the switch 439a and the switch 439b are controlled by the latch pulse.

[0197] When the video signal is a light signal, a signal current is outputted from each current source circuit (current source circuits 437a, 438a, 437b, and 438b) to the pixels. On the other hand, when the video signal is a dark signal, the current source circuits (current source circuits 437a, 438a, 437b, and 438b) have no ability of feeding current, thus feeding no current to the pixels. More specifically, in the current source circuits (current source circuits 437a, 438a, 437b, and 438b), the ability (V_{GS}) of feeding a constant current is controlled by the video signal; thus, the brightness is controlled depending on the magnitude of the current outputted to the pixels.

[0198] The total amount of the current from either of the 1-bit current source circuit 437a and current source circuit 438a and either of the 2-bit current source circuit 437b and current source circuit 438b is carried to the pixels and in the signal lines connected to the pixels.

[0199] Which of the 1-bit current source circuit 437a and current source circuit 438a performs setting operation and which performs inputting operation (output of current to the pixels) are controlled by the latch pulse. The same applies to the 2-bit current source circuit 437b and current source circuit 438b.

[0200] In other words, the currents of the video signals

of the respective bits are combined for DA conversion in the position where the currents flow from the current source circuit 437a and the current source circuit 437b toward the pixels. Therefore, the magnitude of the current has only to correspond to the respective bits.

[0201] Next, the outline of the signal-line drive circuit shown in Fig. 26 will be described. Referring to Fig. 26, the latch circuit includes a switch 435c, a switch 435d, a switch 436c, a current source circuit 437c, a current source circuit 438c, and a switch 439c for each column. The switch 435c and the switch 435d are controlled by the sampling pulses inputted from the shift register 418. The switch 436c and the switch 439c are controlled by the latch pulses.

[0202] To the switch 436c and the switch 439c, inverted signals from each other are inputted. As a result, one of the current source circuit 437c and the current source circuit 438c performs setting operation and the other performs inputting operation. One of the current source circuit 437c and the current source circuit 438c performs setting operation and the other performs inputting operation.

[0203] In other words, when the current source circuit 437a performs setting operation, the current source circuit 438a outputs a signal current to pixels at the same time, thus performing inputting operation. In this manner, since the setting operation and the inputting operation of the current source circuits can be performed at the same time, setting operation can accurately be performed over a long period of time.

[0204] In other words, the setting operation must be continued until a steady state in order to perform the setting operation accurately. Upon the steady state, no current flows to the gate electrode of a transistor (a transistor for supplying a constant current, corresponding to a transistor 102 in Fig. 6A) in the current source circuit, causing no change of the potential of a capacitance (corresponding to a capacitance device 103 in Fig. 6A) that holds the gate-to-source voltage of the transistor. It follows from such a state that setting operation is completed sufficiently. In short, a proper magnitude of current can be fed in inputting operation. However, setting operation of short duration may cause the setting operation to be completed before the steady state. In such a case, the capacitance that holds the gate-to-source voltage of the transistor is not at a correct potential. Therefore, a proper magnitude of current cannot be fed in inputting operation; thus, the circuit is affected by the variations in the characteristics of the transistors. Accordingly, setting operation of long duration allows accurate setting operation.

[0205] Each of the current source circuits 437c and 438c has a terminal a, a terminal b, and a terminal c. Each of the current source circuits 437c and 438c is controlled by a signal inputted through the terminal a, and holds a current (signal current I_{data}) that is set using the video-signal constant current source 109 connected to the video line via the terminal b. The current set in the 1-bit and 2-bit constant current source s 109 is held in the current source circuit 437a or the current source circuit 438a. The switch 439c is arranged between the current source circuits 437a and 438a and the pixels connected to the signal lines, wherein the ON/OFF of the switch 439c is controlled by the latch pulse.

[0206] When the digital video signal is a light signal, signal current is outputted from the current source circuits 437c and 438c to the pixels. On the other hand, when the video signal is a dark signal, the current source circuits 437c and 438c have no ability of feeding current, thus feeding no current to the pixels. In brief, in the current source circuits 437c and 438c, the ability (V_{GS}) of feeding a constant current is controlled by the video signal; thus, the brightness is controlled by the magnitude of the current outputted to the pixels.

[0207] In the present invention, the setting signal inputted from the terminal a indicates a signal inputted from the output terminal of a logical operator. In other words, the setting signal in Fig. 1 corresponds to a signal inputted from the output terminal of the logical operator. In the present invention, the current source circuit 420 is set in accordance with the signal inputted from the output terminal of the logical operator.

[0208] The sampling pulse from the shift register is inputted to one of the two input terminals of the logical operator and the latch pulse is inputted to the other. The logical operator performs logical operation of the two inputted signals and outputs a signal from the output terminal. In the current source circuits, setting operation or inputting operation is performed in accordance with the signal inputted from the output terminal of the logical operator.

[0209] The following is an example of employing a circuit of Fig. 6A as each current source circuit shown in Fig. 5 and each current source circuit shown in Fig. 26. Using the current source circuit as in Fig. 6A decreases the number of transistors to be arranged, thus further reducing the effects of variations in the characteristics of the transistors. In other words, since a transistor for setting operation and a transistor for inputting operation are the identical transistor, they are not affected by the variations between the transistors at all. However, since the current in performing setting operation cannot be set high, setting operation cannot be performed more quickly. The current in setting operation corresponds to the current supplied to the latch circuit from the video-signal constant current source 109.

[0210] A circuit diagram in this case is shown in Fig. 42.

[0211] Subsequently, a case where a current mirror circuit as shown in Fig. 6C is employed as each current source circuit shown in Fig. 5 and each current source circuit shown in Fig. 26 will be described with reference to Fig. 43.

[0212] In the two transistors of the current mirror circuit as in Fig. 6C, when the value of W (gate width)/L (gate length) of the transistor connected to the pixels is

smaller than that of the transistor connected to the video-signal constant current source 109, the current value supplied from the video-signal constant current source 109 can be made high.

[0213] In other words, the value W/L of the transistor for setting operation is set higher than the value W/L of the transistor for inputting operation. Then, the current for setting operation, that is, the current flowing from the video-signal constant current source 109 to the latch circuit can be increased. High current allows electrical charge to be carried quickly to a wiring cross capacitance accompanying wirings, thereby entering a steady state quickly. Thus, setting operation can be performed more quickly.

[0214] The current mirror circuit as in Fig. 6C includes at least two transistors having a gate electrode in common or electrically connected thereto. When the two transistors have identical characteristics, the currents outputted from the source terminals or drain terminals of the transistors do not vary. In brief, the two transistors need to be identical in order not to vary the outputted currents. In other words, it is sufficient for the two transistors having a gate electrode in common or electrically connected thereto to have identical characteristics in the current mirror circuit as in Fig. 6C. Transistors having no common gate electrode do not need to have the identical characteristic. This is because setting operation is performed for each current source circuit. In other words, it is sufficient for the transistor for the setting operation and the transistor used for inputting operation to have the identical characteristics. There is no need for transistors having no common gate electrode to have the identical characteristics. Even when the transistors having no common gate electrode have not identical characteristics, setting operation is performed for each current source circuit; therefore, variations in characteristics are corrected.

[0215] In general, in the current mirror circuit as in Fig. 6C, two transistors having a gate electrode in common or electrically connected thereto are arranged in close proximity to each other in order to reduce the variations in the characteristics thereof.

[0216] Let the magnitude of current applied to the pixels be P. In the two transistors of the current mirror circuit in the current source circuits, if the value W/L of the transistor connected to the pixels is denoted by Wa, the value W/L of the transistor connected to the video signal line is set to (2 x Wa). Then, the current value becomes twice in each current source circuit. Then, the video-signal constant current source s 109 (for 1-bit and 2-bit) supply a current of (2 $\times$ P) or (4 $\times$ P). Consequently, the current supplied from the video-signal constant current source s 109 can be increased, thus allowing the setting operation of each current source circuit to be performed quickly and accurately.

[0217] Since this embodiment performs 2-bit digital intensity-level assigning, it is provided with four current source circuits (437a, 438a, 437b, and 438b) for each signal line in Fig. 5, and two current source circuits (437c and 438c) for each signal line in Fig. 26.

[0218] The current source circuits (current source circuits 437a, 438a, 437b, and 438b) in Fig. 5 and the current source circuits (current source circuits 437c and 438c) shown in Fig. 26 can freely employ the circuit configurations of the current source circuits shown in Figs. 6 and 7, Fig. 29, Fig. 28, and Fig. 31. The current source circuits 420 may adopt not only one system but also a plurality of systems.

[0219] When the current source circuit held in the latch circuit is a current mirror circuit as in Fig. 6C, the value W (gate width)/L (gate length) of the transistor may be varied for each bit. This allows the current in setting operation for a low-order-bit current source circuit, that is, the current flowing from the low-order-bit video-signal constant current source 109 can be made high, leading to a quick setting operation.

[0220] In a word, the value W/L of the transistor connected to the video-signal constant current source 109 is set higher than the W/L of the transistor connected to the pixels and signal lines. In short, the value W/L of the transistor for setting operation is set larger than the value W/L of the transistor for inputting operation. This further increases the current for setting operation, that is, the current flowing from the video-signal constant current source 109.

[0221] However, the current mirror circuit as in Fig. 6C includes at least two transistors having a gate electrode in common or electrically connected thereto. When the two transistors vary in characteristics, the currents outputted therefrom also vary. However, the magnitude of the currents can be varied by setting the ratio W/L of the channel width W and the channel length L of the transistor to different values for the two transistors. Generally, the current in setting operation is set high, thus allowing quick setting operation.

[0222] The current in setting operation corresponds to the current supplied from the video-signal constant current source 109.

[0223] On the other hand, when the circuit as in Fig. 6A is used, the current flowing in setting operation and the current flowing in inputting operation are substantially equal. Therefore, the current for setting operation cannot be set high. However, the transistor for supplying current in setting operation and the transistor for supplying current in inputting operation are the identical. Therefore, they are not affected by the variations between the transistors at all. Accordingly, it is preferable to use an appropriate combination in the latch circuit, such as to use the current mirror circuit as in Fig. 6C for part where high current is desired in setting operation and to use the circuit as in Fig. 6A for part where more accurate current is desired to output.

[0224] The current mirror circuit as in Fig. 6C includes at least two transistors having a gate electrode in common or electrically connected thereto. When the two transistors vary in characteristics, the currents outputted

therefrom also vary. However, if the two transistors have identical characteristics, the currents outputted from the source terminals or drain terminals of the transistors do not vary. Conversely, the characteristics of the two transistors need to be identical in order not to vary the outputted currents. In other words, in the current mirror circuit as in Fig. 6C, it is sufficient for the two transistors having a gate electrode in common or electrically connected thereto to have identical characteristics. Transistors having no common gate electrode do not need to have the identical characteristic. This is because setting operation is performed for each current source circuit. In other words, it is sufficient for the transistor for the setting operation and the transistor used for inputting operation to have the identical characteristics. Even when the transistors having no common gate electrode have not identical characteristics, setting operation is performed for each current source circuit; therefore, variations in characteristics are corrected.

[0225] In general, in the current mirror circuit as in Fig. 6C, two transistors having a gate electrode in common or electrically connected thereto are arranged in close proximity to each other in order to reduce the variations in the characteristics of the two transistors.

[0226] The current source circuit held in the latch circuit may employ the circuit as in Fig. 6A or the current mirror circuit as in Fig. 6C, or alternatively, may employ a combination thereof.

[0227] The current mirror circuit as in Fig. 6C may be adopted in either a current source circuit for all bits or a current source circuit for part of bits. More effectively, it is preferable to use the current mirror circuit as in Fig. 6C for the low-order-bit current source circuit and to use the circuit as in Fig. 6A for the high-order-bit current source circuit.

[0228] This is because the high-order-bit current source circuit affects the current value significantly even if the characteristics of the transistors in the current source circuit vary slightly; this is because the absolute value of the difference in current due to the variations is large even with the same degree of variations in the characteristics of the transistors since the current supplied from the high-order-bit current source circuit is high in itself. Assuming that the characteristics of the transistors vary by ten percent, the amount of variations is 0.1I where the magnitude of the first-bit current is I. On the other hand, since the magnitude of the third-bit current amounts to 8I, the amount of the variations is 0.8I. As just described, even a slight variation in the characteristics of the transistors significantly affects the high-order-bit current source circuit.

[0229] Therefore, a system that is affected by the variations as little as possible is preferable. The high-order-bit current has a high current value, facilitating setting operation. On the other hand, the low-order-bit current exhibits a low value of current itself despite of some variations, having slight influence. Also, since the low-order-bit current exhibits a low value of current, setting operation is not easy.

[0230] In order to resolve the above situations, it is preferable to use the current mirror circuit as in Fig. 6C for the low-order-bit current source circuit and to use the circuit as in Fig. 6A for the high-order-bit current source circuit.

[0231] Particularly, for the low-order-bit current source circuit in which the current flowing from the video-signal constant current source 109 is low, it is effective to use the current mirror circuit as in Fig. 6C to increase the value of current.

[0232] More specifically, the low-order-bit current source circuit exhibits a low value of current flowing therefrom, thus taking much time for setting operation. Therefore, increasing the current value using the current mirror circuit as in Fig. 6C decreases the time for setting operation.

[0233] The current mirror circuit as in Fig. 6C includes at least two transistors having a gate electrode in common or electrically connected thereto. When the two transistors vary in characteristics, the currents outputted therefrom also vary. However, the low-order-bit current source circuit exhibits a low value of current outputted to the pixels and the signal lines. Therefore, variations in the characteristics of the two transistors have little effects. Therefore, it is effective for the low-order-bit current source circuit to use the current mirror circuit as in Fig. 6C.

[0234] In summary, by employing the current mirror circuit as in Fig. 6C as a current source circuit and setting the value W/L to an appropriate value, the current to be supplied from the video-signal constant current source 109 can be made high. This allows the setting operation of the current source circuit to be performed accurately.

[0235] However, the current mirror circuit as in Fig. 6C includes at least two transistors having a gate electrode in common or electrically connected thereto. If the two transistors vary in characteristics, the currents outputted therefrom also vary.

[0236] On the other hand, when the circuit as in Fig. 6A is used, the current flowing in setting operation cannot be increased; however, which is not at all affected by the variations between the transistors.

[0237] Accordingly, it is preferable to use a combination of circuits appropriately, as to use the current mirror circuit as in Fig. 6C for part where high current is desired and to use the circuit as in Fig. 6A for part where more accurate current is desired to output.

[0238] The transistor to be operated as merely a switch may have either polarity.

[0239] Referring to Fig. 5, the 1-bit video-signal constant current source 109 is connected to a 1-bit video line (video data line) and the 2-bit video-signal constant current source 109 is connected to a 2-bit video line (video data line). Assuming that current supplied from the 1-bit video-signal constant current source 109 is I, current supplied from the 2-bit video-signal constant cur-

rent source 109 is 2I. However, the present invention is not limited to that but the magnitude of the currents supplied from the 1-bit video-signal constant current source 109 and the 2-bit video-signal constant current source 109 can be equated. Equating the magnitude of the currents supplied from the 1-bit video-signal constant current source 109 and the 2-bit video-signal constant current source 109 allows the operating conditions and the load to be equated and also the time for writing signals to the current source circuits to be the same.

[0240] However, at that time, the current source circuits shown in Fig. 5 and Fig. 26 need to employ the current mirror circuit as in Fig. 6C. In the current source circuits shown in Fig. 5, it is necessary to set the values W/L of the transistors held in the current source circuit 437a and the current source circuit 438a and the transistors held in the current source circuit 437b and the current source circuit 438b to 2:1. Thus, the ratio of the magnitude of the current outputted from the current source circuit 437a and the current source circuit 438a and the magnitude of the current outputted from the current source circuit 437b and the current source circuit 438b can be set to 2:1. In the current source circuits shown in Fig. 26, the value W/L of the transistors connected to the video signal lines and the transistors connected to the pixels must be 2:1.

[0241] In this embodiment, the configuration and the operation of the signal-line drive circuit for performing 2-bit digital intensity-level assigning are described. However, according to the present invention, a signal-line drive circuit ready for not only the 2-bit but for any-bit can be designed on the basis of this embodiment to perform arbitrary bit assigning. This embodiment can freely be combined with the first to fourth embodiments.

[Sixth Embodiment]

[0242] The video-signal constant current source 109 shown in Fig. 2 to Fig. 5 may be integrated with the signal-line drive circuit on the substrate, or alternatively, may be arranged outside the substrate, from which a certain current is inputted using an IC and so on. For integral formation on the substrate, either of the current source circuits shown in Figs. 6 to 8, Fig. 29, Fig. 28, and Fig. 31 may be used. Alternatively, only one transistor may be arranged to control the current value depending on the voltage to be applied to the gate. In this embodiment, a case in which a 3-bit video-signal constant current source 109 is configured with the current source circuit of the current mirror circuit as in Fig. 6C will be described with reference to Fig. 23 to Fig. 25.

[0243] The direction in which the current flows varies depending on the configuration of pixels. Changing the direction of the flow of current can easily be prepared by changing the polarity of the transistor.

[0244] Referring to Fig. 23, the video-signal constant current source 109 controls whether to output a predetermined signal current I_{data} to a video line (a video data line and a current line) in accordance with the information on High/Low held in the 3-bit digital video signals (digital data 1 to digital data 3)

[0245] The video-signal constant current source 109 includes a switch 180 to a switch 182, a transistor 183 to a transistor 188, and a capacitance device 189. In this embodiment, all the transistor 180 to the transistor 188 are of n-channel type.

[0246] The switch 180 is controlled by a 1-bit digital video signal. The switch 181 is controlled by a 2-bit digital video signal. The switch 183 is controlled by a 3-bit digital video signal.

[0247] One of the source area and the drain area of the transistor 183 to the transistor 185 is connected to Vss and the other is connected to one of the terminals of the switch 180 to the switch 182. One of the source area and the drain area of the transistor 186 is connected to Vss and the other is connected to one of the source area and the source area of the transistor 188.

[0248] A signal is inputted from the exterior to the respective gate electrodes of the transistor 187 and the transistor 188 via a terminal e. To a current line 190, current is supplied from the exterior via a terminal f.

[0249] One of the source area and the drain area of the transistor 187 is connected to one of the source area and the drain area of the transistor 186 and the other is connected to one electrode of the capacitance device 189. One of the source area and the drain area of the transistor 188 is connected to the current line 190 and the other is connected to one of the source area and the drain area of the transistor 186.

[0250] One electrode of the capacitance device 189 is connected to the gate electrodes of the transistor 183 to the transistor 186 and the other electrode is connected to Vss. The capacitance device 189 is responsible for holding the gate-to-source voltage of the transistor 183 to the transistor 186.

[0251] In the video-signal constant current source 109, when the transistor 187 and the transistor 188 are turned on by the signal inputted from the terminal e, the current supplied from the terminal f is carried to the capacitance device 189 over the current line 190.

[0252] Electrical charge is gradually stored in the capacitance device 189 to begin generating a potential difference between both electrodes. When the potential difference between both electrodes reaches V_{th}, the transistor 183 to the transistor 186 are turned on.

[0253] In the capacitance device 189, the storage of electrical charge is continued until the potential difference between both electrodes, that is, the gate-to-source voltage of the transistor 183 to the transistor 186 reaches a desired voltage. In other words, the storage of electrical charge is continued until a voltage at which the transistor 183 to the transistor 186 can feed signal current can be obtained.

[0254] After completion of the storage of electrical charge, the transistor 183 to the transistor 186 are fully tuned on.

[0255] In the video-signal constant current source 109, continuity or discontinuity of the switch 180 to the switch 182 is selected according to the 3-bit digital signal. For example, when all the switch 180 to the switch 182 come in continuity, a current supplied to the current lines is the total amount of the drain current of the transistor 183, the drain current of the transistor 184, and the drain current of the transistor 185. When only the switch 180 comes in continuity, only the drain current of the transistor 183 is supplied to the current line.

[0256] When the ratio of the drain current of the transistor 183, the drain current of the transistor 184, and the drain current of the transistor 185 is set at 1:2:4, the magnitude of the current can be controlled in the level of $2^3 = 8$. Therefore, when the values W (channel width) /L (channel length) of the transistor 183 to the transistor 185 are designed at 1:2:4, the ratio of the respective ON-state currents reaches 1:2:4.

[0257] Fig. 23 shows a configuration with one current line (video line). However, the number of current lines (video lines) to be arranged differs depending on whether the circuit as in Fig. 4 or the circuit as in Fig. 26 is used. Fig. 44 shows a diagram when a plurality of current lines (video lines) is used in the circuit of Fig. 23.

[0258] Next, the video-signal current source 109 with a different configuration from that of Fig. 23 is shown in Fig. 24. In Fig. 24, when compared to the video-signal current source 109 shown in Fig. 23, the operation is the same as that of the video-signal current source 109 shown in Fig. 23 except that the transistors 187 and 188 are eliminated and one terminal of the capacitance device 189 is connected to the current line 190; therefore, a description thereof will be omitted in this embodiment.

[0259] With the configuration of Fig. 24, the signal (current) must continuously be inputted through the terminal f while current is supplied to the video line (current line). If the input of the current flowing from the terminal f is stopped, the electrical charge in the capacitance device 189 is discharged through the transistor 186. Consequently, the potential of the gate electrode of the transistor 186 is decreased to avoid the output of normal current from the transistors 183 to 185. On the other hand, with the configuration of Fig. 23, the capacitance device 189 holds a predetermined electrical charge; therefore, there is no need to input the signal (current) through the terminal f continuously while current is supplied to the video line (current line). Therefore, the capacitance device 189 may be omitted in the configuration of Fig. 24.

[0260] Fig. 24 shows a configuration with one current line (video line). However, the number of current lines (video lines) differs depending on whether the circuit as in Fig. 4 or the circuit as in Fig. 26 is used. Thus, Fig. 45 shows a diagram when a plurality of current lines (video lines) is used in the circuit in Fig. 24.

[0261] Subsequently, the video-signal current source 109 with a different configuration from those of Figs. 23 and 24 will be shown in Fig. 25. In Fig. 25, as compared to the video-signal current source 109 shown in Fig. 23, the operation is the same as that of the video-signal current source 109 shown in Fig. 23 except that the transistors 186, 187, and 188 and the capacitance device 189 are eliminated, and a constant voltage is applied from the exterior to the gate electrodes of the transistor 183 to the transistor 185 via the terminal f; therefore, a description thereof will be omitted in this embodiment.

[0262] In the case of Fig. 25, voltage (gate voltage) is applied to the gate electrodes of the transistors 183 to 185 through the terminal f. However, even if the same gate voltage is applied to the transistors 183 to 185, the values of the current flowing between the source and the drain of the transistors 183 to 185 vary with the variations in the characteristics of the transistors 183 to 185. Accordingly, current flowing in the video line (current line) also varies. Also, since the characteristics vary by temperature, the values of currents supplied from the transistors 183 to 185 vary as well.

[0263] On the other hand, in the case of Fig. 23 and Fig. 24, current as well as voltage can be applied through the terminal f. When current is applied, the value of current does not vary if the transistors 183 to 186 have the identical characteristics. Even if the characteristics vary by temperature, the characteristics of the transistors 183 to 186 also vary at the same level as that; thus, the current value does not vary.

[0264] In Fig. 25, voltage (gate voltage) is applied to the transistors 183 to 185 through the terminal f, which does not vary by the video signal. In Fig. 25, the video signal controls whether current flows in the current line by controlling the switches 180 to 182. Therefore, as in Fig. 46, voltage (gate voltage) is applied to the gate electrodes of the transistors 183 to 185, wherein the voltage may be varied by the video signal. Thus, the magnitude of the video-signal current can be varied. Also, as in Fig. 47, voltage (gate voltage) applied to the gate electrode of the transistor 183 may be analog voltage, wherein the voltage and thus current may be varied depending on the gray level.

[0265] Subsequently, the video-signal current source 109 with a different configuration from those of Figs 23, 24, and 25 is shown in Fig. 9. While, Fig. 23 employed the current source circuit of Fig. 6C, Fig. 9 employs the current source circuit of Fig. 6A.

[0266] In the case of Fig. 23, when the characteristics of the transistors 183 to 186 vary, the current values also vary. On the other hand, in Fig. 9, setting operation is performed for each current source , thus reducing the effects of the variations of the transistors. However, in the case of Fig. 9, inputting operation (operation of supplying current to the current line) cannot be performed simultaneously with the setting operation. Accordingly, the setting operation must be performed during the period of time the inputting operation is not performed. In order to allow the setting operation to be performed also during the inputting operation, a plurality of current source circuits may be arranged, as in Fig. 10, so that

while one current source circuit performs the setting operation, the other current source circuit can perform the inputting operation.

[0267] This embodiment may freely be combined with the first to fifth embodiments.

[Seventh Embodiment]

[0268] An embodiment of the present invention will be described with reference to Fig. 11. Referring to Fig. 11A, a signal-line drive circuit is disposed above a pixel section; and a constant current circuit is disposed below, wherein a current source A is disposed in the signal-line drive circuit and a current source B is disposed in the constant current circuit. Equation $I_A = I_B + I_{data}$ is established where currents supplied from the current source s A and B are I_A and I_B, respectively, and signal current supplied to the pixels is I_{data}. Setting is made so that currents are supplied from both current source s A and B when signal current is written into the pixels. At that time, increasing I_A and I_B can increase the writing speed of the signal current to the pixels.

[0269] At that time, the setting operation for the current source B is performed using the current source A. Current that is obtained by subtracting the current of the current source B from the current fed from the current source A flows to the pixels. Therefore, the setting operation for the current source B using the current source A can reduce the effects of noise and so on.

[0270] Referring to Fig. 11B, video-signal constant current source s (hereinafter, referred to as constant current source s) C and E are arranged above and below the pixel section, respectively. Setting operation for the current source circuits disposed in the signal-line drive circuit and the constant current circuit is performed using the current source s C and E. A current source D serves as a current source for setting the current source s C and E, to which video-signal current is supplied from the exterior.

[0271] In Fig. 11B, the constant current circuit arranged below may be a signal-line drive circuit. This allows the video-signal drive circuits to be arranged both above and below, which control the upper and lower half of a screen (the whole pixel section), respectively. With such an arrangement, two columns of pixels can simultaneously be controlled. Therefore, the time for setting operation (signal inputting operation) for the current source s of the signal-line drive circuit, the pixels, and the current source s for the pixels can be increased, thus allowing more accurate setting.

[0272] This embodiment can freely be combined with the first to sixth embodiments.

Examples

[Example 1]

[0273] In this example, the time gradation method will be described in detail with reference to Fig. 14. In display devices such as liquid crystal display devices and light emitting devices, a frame frequency is about 60 (Hz). That is, as shown in Fig. 14A, screen rendering is performed about 60 times per second. This enables flickers (flickering of a screen) not to be recognized by the human eyes. At this time, a period during which screen rendering is performed once is called one frame period.

[0274] As an example, in Example 1, a description will be made of a time gradation method disclosed in the publication as Patent Document 1. In the time gradation method, one frame period is divided into a plurality of subframe periods. In many cases, the number of divisions is identical to the number of gradation bits. For the sake of a simple description, a case where the number of divisions is identical to the number of gradation bits. Specifically, since the 3-bit gradation is employed in this example, an example is shown in which one frame period is divided into three subframe periods SF1 to SF3 (Fig. 14B).

[0275] Each of the subframe periods includes an address (writing) period Ta and a sustain (light emission) period (Ts). The address period is a period during which a video signal is written to a pixel, and the length thereof is the same among respective subframe periods. The sustain period is a period during which the light emitting element emits light in response to the video signal written in the address period Ta. At this time, the sustain periods SF1 to SF3 are set at a length ratio of Ts1 : Ts2 : Ts3 = 4 : 2 : 1. More specifically, the length ratio of n sustain periods is set to $2^{(n-1)} : 2^{(n-2)} : \ldots : 2^1 : 2^0$. Depending on whether a light emitting element performs emission in which one of the sustain periods, the length of the period during which each pixel emits light in one frame period is determined, and the gradation representation is thus performed.

[0276] Next, a specific operation of a pixel employing the time gradation method will be described. In this example, a description thereof will be made referring to the pixel shown in Fig. 16B. A current input method is applied to the pixel shown in Fig. 16B.

[0277] First, the following operation is performed during the address period Ta. A first scanning line 602 and a second scanning line 603 are selected, and TFTs 606 and 607 are turned ON. A current flowing through a signal line 601 at this time is used as a signal current I_{data}. Then, when a predetermined charge has been accumulated in a capacitor device 610, selection of the first and second scanning lines 602 and 603 is terminated, and the TFTs 606 and 607 are turned OFF.

[0278] Subsequently, the following operation is performed in the sustain period Ts. A scanning line 604 is selected, and a TFT 609 is turned ON. Since the predetermined charge that has been written is stored in the capacitor device 610, the TFT 608 is already turned ON, and a current identical with the signal current I_{data} flows thereto from a current line 605. Thus, a light emitting element 611 emits light.

[0279] The operations described above are performed in each subframe period, thereby forming one frame period. According to this method, the number of divisions for subframe periods may be increased to increase the number of display gradations. The order of the subframe periods does not necessarily need to be the order from an upper bit to a lower bit as shown in Figs. 14B and 14C, and the subframe periods may be disposed at random within one frame period. In addition, the order may be variable within each frame period.

[0280] Further, a subframe period SF2 of an m-th scanning line is shown in Fig. 14D. As shown in Fig. 14D, in the pixel, upon termination of an address period Ta2, a sustain period Ts2 is immediately started.

[0281] This example may be arbitrarily combined with Embodiments 1 to 7.

[Example 2]

[0282] In this example, example structures of pixel circuits provided in the pixel portion will be described with reference to Fig. 13.

[0283] Note that a pixel of any structure may be applicable as long as the structure includes a current input portion.

[0284] A pixel shown in Fig. 13A includes a signal line 1101, first and second scanning lines 1102 and 1103, a current line (power supply line) 1104, a switching TFT 1105, a holding TFT 1106, a driving TFT 1107, a conversion driving TFT 1108, a capacitor device 1109, and a light emitting element 1110. Each signal line is connected to a current source circuit 1111.

[0285] Note that the current source circuit 1111 corresponds to the current source circuit 420 disposed in the signal line drive circuit 403.

[0286] The gate electrode of the switching TFT 1105 is connected to the first scanning line 1102, a first electrode thereof is connected to the signal line 1101, and a second electrode thereof is connected to a first electrode of the driving TFT 1107 and a first electrode of the conversion driving TFT 1108. The gate electrode of the holding TFT 1106 is connected to the second scanning line 1103, a first electrode thereof is connected to the signal line 1102, and a second electrode thereof is connected to the gate electrode of the driving TFT 1107 and the gate electrode of the conversion driving TFT 1108. A second electrode of the driving TFT 1107 is connected to the current line (power supply line) 1104, and a second electrode of the conversion driving TFT 1108 is connected to one of the electrodes of the light emitting element 1110. The capacitor device 1109 is connected between the gate electrode of the conversion driving TFT 1108 and a second electrode thereof, and retains a gate-source voltage of the conversion driving TFT 1108. The current line (power supply line) 1104 and the other electrode of the light emitting element 1110 are respectively input with predetermined potentials and have mutually different potentials.

[0287] The pixel of Fig. 13A corresponds to the case where a circuit of Fig. 29B is applied to a pixel. However, since the current-flow direction is different, the transistor polarity is reverse. The driving TFT 1107 of Fig. 13A corresponds to a TFT 126 of Fig. 29B, the conversion driving TFT 1108 of Fig. 13A corresponds to a TFT 122 of Fig. 29B, and the holding TFT 1106 of Fig. 13A corresponds to the TFT 124 of Fig. 29B.

[0288] A pixel shown in Fig. 13B includes a signal line 1151, first and second scanning lines 1142 and 1143, a current line (power supply line) 1144, a switching TFT 1145, a holding TFT 1146, a conversion driving TFT 1147, a driving TFT 1148, a capacitor device 1149, and a light emitting element 1140. The signal line 1151 is connected to a current source circuit 1141.

[0289] Note that the current source circuit 1141 corresponds to the current source circuit 420 disposed in the signal line drive circuit 403.

[0290] The gate electrode of the switching TFT 1145 is connected to the first scanning line 1142, a first electrode thereof is connected to the signal line 1151, and a second electrode thereof is connected to a first electrode of the driving TFT 1148 and a first electrode of the conversion driving TFT 1148. The gate electrode of the holding TFT 1146 is connected to the second scanning line 1143, a first electrode thereof is connected to the first electrode of the drive TFT 1148, and a second electrode thereof is connected to the gate electrode of the driving TFT 1148 and the gate electrode of the conversion driving TFT 1147. A second electrode of the conversion driving TFT 1147 is connected to the current line (power supply line) 1144, and a second electrode of the conversion driving TFT 1147 is connected to one of the electrodes of the light emitting element 1140. The capacitor device 1149 is connected between the gate electrode of the conversion driving TFT 1147 and a second electrode thereof, and retains a gate-source voltage of the conversion driving TFT 1147. The current line (power supply line) 1144 and the other electrode of the light emitting element 1140 are respectively input with predetermined potentials and have mutually different potentials.

[0291] Note that the pixel of Fig. 13B corresponds to the case where a circuit of Fig. 6B is applied to a pixel. However, since the current-flow direction is different, the transistor polarity is reverse. The conversion driving TFT 1147 of Fig. 13B corresponds to a TFT 122 of Fig. 6B, the driving TFT 1138 of Fig. 13B corresponds to a TFT 126 of Fig. 6B, and the holding TFT 1136 of Fig. 13B corresponds to the TFT 124 of Fig. 6B.

[0292] A pixel shown in Fig. 13C includes a signal line 1121, a first scanning line 1122, a second scanning line 1123, a third scanning line 1135, a current line (power supply line) 1124, a current line 1138, a switching TFT 1125, an erasing TFT 1126, a driving TFT 1127, a capacitor device 1128, a current-supply TFT 1129, a mirror TFT 1130, a capacitor device 1131, a current-input TFT 1132, a holding TFT 1133, and a light emitting element

1136. Each signal line is connected to a current source circuit 1137.

[0293] The gate electrode of the switching TFT 1125 is connected to the first scanning line 1122, a first electrode of the switching TFT 1125 is connected to the signal line 1121, and a second electrode of the switching TFT 1125 is connected to the gate electrode of the driving TFT 1127 and a first electrode of the erasing TFT 1126. The gate electrode of the erasing TFT 1126 is connected to the second scanning line 1123, and a second electrode of the erasing TFT 1126 is connected to the current line (power supply line) 1124. A first electrode of the driving TFT 1127 is connected to one of the electrodes of the light emitting element 1136, and a second electrode of the driving TFT 1127 is connected to a first electrode of the current-supply TFT 1129. A second electrode of the current-supply TFT 1129 is connected to the current line (power supply line) 1124. One of the electrodes of the capacitor device 1131 is connected to the gate electrode of the current-supply TFT 1129 and the gate electrode of the mirror TFT 1130 and the other electrode thereof is connected to the current line (power supply line) 1124. A first electrode of the mirror TFT 1130 is connected to the current line 1124, and a second electrode of the mirror TFT 1130 is connected to a first electrode of the current-input TFT 1132. A second electrode of the current-input TFT 1132 is connected to the current line (power supply line) 1124, and the gate electrode of the current-input TFT 1132 is connected to the third scanning line 1135. The gate electrode of the current holding TFT 1133 is connected to the third scanning line 1135, a first electrode of the current holding TFT 1133 is connected to the pixel current line 1138, a second electrode of the current holding TFT 1133 is connected to the gate electrode of the current-supply TFT 1129 and the gate electrode of the mirror TFT 1130. The current line (power supply line) 1124 and the other electrode of light emitting element 1136 are input with predetermined potentials and have mutually different potentials.

[0294] This example may be arbitrarily combined with Embodiments 1 to 7 and Example 1.

[Example 3]

[0295] In this example, technical devices when performing color display will be described.

[0296] With a light emitting element comprised of an organic EL element, the luminance can be variable depending on the color even though a current having the same magnitude is supplied to the light emitting device. In addition, in the case where the light emitting element has deteriorated because of, for example, a time factor, the deterioration degree is variable depending on the color. Thus, when performing color display with a light emitting device using light emitting elements, various technical devices are required to adjust the white balance.

[0297] The simplest technique is to change the magnitude of the current that is input to the pixel. To achieve the technique, the magnitude of the video-signal current source should be changed depending on the color.

[0298] Another technique is to use circuits as shown in Figs. 6C to 6E for the pixel, signal line drive circuit, video-signal current source , and the like. In the circuits as shown in Figs. 6C to 6E, the W/L ratio of two transistors forming the current mirror circuit is changed depending on the color. Thus, the magnitude of the current to be input to the pixel can be changed depending on the color.

[0299] Still another technique is to change the length of a lightening period. The technique can be applied to either of the case where the time gradation method is employed and the case where the time gradation method is not employed. According to the technique, the luminance of each pixel can be adjusted.

[0300] The white balance can be easily adjusted by using any one of the techniques or a combination thereof.

[0301] This example may be arbitrarily combined with Embodiments 1 to 7 and Examples 1 and 2.

[Example 4]

[0302] In this example, the appearances of the light emitting devices (semiconductor devices) of the present invention will be described using Fig. 12. Fig. 12A is a top view of a light emitting device formed such that an element substrate on which transistors are formed is sealed with a sealing material; Fig. 12B is a cross-sectional view taken along the line A-A' of Fig. 12A; and Fig. 12C is a cross-sectional view taken along the line B-B' of Fig. 12A.

[0303] A sealing material 4009 is provided so as to enclose a pixel portion 4002, a source signal line drive circuit 4003, and gate signal line drive circuits 4004a and 4004b that are provided on a substrate 4001. In addition, a sealing material 4008 is provided over the pixel portion 4002, the source signal line drive circuit 4003, and the gate signal line drive circuits 4004a and 4004b. Thus, the pixel portion 4002, the source signal line drive circuit 4003, and the gate signal line drive circuits 4004a and 4004b are sealed by the substrate 4001, the sealing material 4009, and the sealing material 4008 with a filler material 4210.

[0304] The pixel portion 4002, the source signal line drive circuit 4003, and the gate signal line drive circuits 4004a and 4004b, which are provided over the substrate 4001, include a plurality of TFTs. Fig. 12B representatively shows a driving TFT (incidentally, an n-channel TFT and a p-channel TFT are shown in this example) 4201 included in the source signal line drive circuit 4003, and an erasing TFT 4202 included in the pixel portion 4002, which are formed on a base film 4010.

[0305] In this example, a p-channel TFT or an n-channel TFT that is manufactured according to a known method is used for the driving TFT 4201, and an n-chan-

nel TFT manufactured according to a known method is used for the erasing TFT 4202.

[0306] An interlayer insulating film (leveling film) 4301 is formed on the driving TFT 4201 and the erasing TFT 4202, and a pixel electrode (anode) 4203 for being electrically connected to a drain of the erasing TFT 4202 is formed thereon. A transparent conductive film having a large work function is used for the pixel electrode 4203. For the transparent conductive film, a compound of indium oxide and tin oxide, a compound of indium oxide and zinc oxide, zinc oxide, tin oxide, or indium oxide can be used. Alternatively, the transparent conductive film added with gallium may be used.

[0307] An insulating film 4302 is formed on the pixel electrode 4203, and the insulating film 4302 is formed with an opening portion formed on the pixel electrode 4203. In the opening portion, a light emitting layer 4204 is formed on the pixel electrode 4203. The light emitting layer 4204 may be formed using a known light emitting material or inorganic light emitting material. As the light emitting material, either of a low molecular weight (monomer) material and a high molecular weight (polymer) material may be used.

[0308] As a forming method of the light emitting layer 4204, a known vapor deposition technique or coating technique may be used. The structure of the light emitting layer 4204 may be either a laminate structure, which is formed by arbitrarily combining a hole injection layer, a hole transportation layer, a light-emitting layer, an electron transportation layer, and an electron injection layer, or a single-layer structure.

[0309] Formed on the light emitting layer 4204 is a cathode 4205 formed of a conductive film (representatively, a conductive film containing aluminum, copper, or silver as its main constituent, or a laminate film of the conductive film and another conductive film) having a light shielding property. Moisture and oxygen existing on an interface of the cathode 4205 and the light emitting layer 4204 are desirably eliminated as much as possible. For this reason, a technical device is necessary in which the light emitting layer 4204 is formed in an nitrogen or noble gas atmosphere, and the cathode 4205 is formed without being exposed to oxygen, moisture, and the like. In this example, the above-described film deposition is enabled using a multi-chamber method (cluster-tool method) film deposition apparatus. In addition, the cathode 4205 is applied with a predetermined voltage.

[0310] In the above-described manner, a light emitting element 4303 constituted by the pixel electrode (anode) 4203, the light emitting layer 4204, and the cathode 4205 is formed. A protective film is formed on the insulating film so as to cover the light emitting element 4303. The protective film is effective for preventing, for example, oxygen and moisture, from entering the light emitting element 4303.

[0311] Reference numeral 4005a denotes a drawing line that is connected to a power supply line and that is electrically connected to a source region of the erasing TFT 4202. The drawing line 4005a is passed between the sealing material 4009 and the substrate 4001 and is then electrically connected to an FPC line 4301 of an FPC 4006 via an anisotropic conductive film 4300.

[0312] As the sealing material 4008, a glass material, a metal material (representatively, a stainless steel material), ceramics material, or a plastic material (including a plastic film) may be used. As the plastic material, an FRP (fiberglass reinforced plastics) plate, a PVF (polyvinyl fluoride) film, a Mylar film, a polyester film, or an acrylic resin film may be used. Alternatively, a sheet having a structure in which an aluminum foil is sandwiched by the PVF film or the Mylar film may be used.

[0313] However, a cover material needs to be transparent when light emission is directed from the light emitting layer to the cover material. In this case, a transparent substance such as a glass plate, a plastic plate, a polyester film, or an acrylic film, is used.

[0314] Further, for the filler material 4210, ultraviolet curing resin or a thermosetting resin may be used in addition to an inactive gas, such as nitrogen or argon; and PVC (polyvinyl chloride), acrylic, polyimide, epoxy resin, silicon resin, PVB (polyvinyl butyral), or EVA (ethylene vinyl acetate) may be used. In this example, nitrogen was used for the filler material.

[0315] To keep the filler material 4210 to be exposed to a hygroscopic substance (preferably, barium oxide) or an oxygen-absorbable substance, a concave portion 4007 is provided on the surface of the sealing material 4008 on the side of the substrate 4001, and a hygroscopic substance or oxygen-absorbable substance 4207 is disposed. The hygroscopic substance or oxygen-absorbable substance 4207 is held in the concave portion 4007 via a concave-portion cover material 4208 such that the hygroscopic substance or oxygen-absorbable substance 4207 does not diffuse. The concave-portion cover material 4208 is in a fine mesh state and is formed to allow air and moisture to pass through and not to allow the hygroscopic substance or oxygen-absorbable substance 4207 to pass through. The provision of the hygroscopic substance or oxygen-absorbable substance 4207 enables the suppression of deterioration of the light emitting element 4303.

[0316] As shown in Fig. 12C, simultaneously with the formation of the pixel electrode 4203, a conductive film 4203a is formed so as to be contact with an upper portion of the drawing line 4005a.

[0317] In addition, the anisotropic conductive film 4300 includes a conductive filler 4300a. The substrate 4001 and the FPC 4006 are thermally press-bonded, whereby the conductive film 4203a on the substrate 4001 and the FPC line 4301 on the FPC 4006 are electrically connected via the conductive filler 4300a.

[0318] This example may be arbitrarily combined with Embodiments 1 to 7 and Examples 1 to 3.

[Example 5]

[0319] A light emitting device using a light emitting element is of self-light emitting type, so that in comparison to a liquid crystal display, the light emitting device offers a better visibility in bright portions and a wider view angle. Hence, the light emitting device can be used in display portions of various electronic device.

[0320] Electronic device using the light emitting device of the present invention include, for example, video cameras, digital cameras, goggle type displays (head mount displays), navigation systems, audio reproducing devices (such as car audio and audio components), notebook personal computers, game machines, mobile information terminals (such as mobile computers, mobile telephones, portable game machines, and electronic books), and image reproducing devices provided with a recording medium (specifically, devices for reproducing a recording medium such as a digital versatile disc (DVD), which includes a display capable of displaying images). In particular, in the case of mobile information terminals, since the degree of the view angle is appreciated important, the terminals preferably use the light emitting device. Practical examples thereof are shown in Fig. 22.

[0321] Fig. 22A shows a light emitting device, which contains a casing 2001, a support base 2002, a display portion 2003, a speaker portion 2004, a video input terminal 2005, and the like. The light emitting device of the present invention can be applied to the display portion 2003. Further, the light emitting device shown in Fig. 22A is completed with the present invention. Since the light emitting device is of self-light emitting type, it does not need a back light, and therefore a display portion that is thinner than a liquid crystal display can be obtained. Note that light emitting devices include all information display devices, for example, personal computers, television broadcast transmitter-receivers, advertisement displays and the like.

[0322] Fig. 22B shows a digital still camera, which contains a main body 2101, a display portion 2102, an image receiving portion 2103, operation keys 2104, an external connection port 2105, a shutter 2106, and the like. The light emitting device of the present invention can be applied to the display portion 2102. Further, the digital still camera shown in Fig. 22B is completed with the present invention.

[0323] Fig 22C shows a notebook personal computer, which contains a main body 2201, a casing 2202, a display portion 2203, a keyboard 2204, external connection ports 2205, a pointing mouse 2206, and the like. The light emitting device of the present invention can be applied to the display portion 2203. Further, the light emitting device shown in Fig. 22C is completed with the present invention.

[0324] Fig 22D shows a mobile computer, which contains a main body 2301, a display portion 2302, a switch 2303, operation keys 2304, an infrared port 2305, and the like. The light emitting device of the present invention can be applied to the display portion 2303. Further, the mobile computer shown in Fig. 22D is completed with the present invention.

[0325] Fig 22E shows a portable image reproducing device provided with a recording medium (specifically, a DVD reproducing device), which contains a main body 2401, a casing 2402, a display portion A 2403, a display portion B 2404, a recording medium (such as a DVD) read-in portion 2405, operation keys 2406, a speaker portion 2407, and the like. The display portion A 2403 mainly displays image information, and the display portion B 2404 mainly displays character information. The light emitting device of the present invention can be used in the display portion A 2403 and in the display portion B 2404. Note that family game machines and the like are included in the image reproducing devices provided with a recording medium. Further, the DVD reproducing device shown in Fig. 22E is completed with the present invention.

[0326] Fig 22F shows a goggle type display (head mounted display), which contains a main body 2501, a display portion 2502, an arm portion 2503, and the like. The light emitting device of the present invention can be used in the display portion 2502. The goggle type display shown in Fig.22 F is completed with the present invention.

[0327] Fig. 22G shows a video camera, which contains a main body 2601, a display portion 2602, a casing 2603, external connection ports 2604, a remote control reception portion 2605, an image receiving portion 2606, a battery 2607, an audio input portion 2608, operation keys 2609, an eyepiece portion 2610, and the like. The light emitting device of the present invention can be used in the display portion 2602. The video camera shown in Fig.22 G is completed with the present invention.

[0328] Here, Fig. 22H shows a mobile telephone, which contains a main body 2701, a casing 2702, a display portion 2703, an audio input portion 2704, an audio output portion 2705, operation keys 2706, external connection ports 2707, an antenna 2708, and the like. The light emitting device of the present invention can be used in the display portion 2703. Note that, by displaying white characters on a black background, the display portion 2703 can suppress the consumption current of the mobile telephone. Further, the mobile telephone shown in Fig. 22H is completed with the present invention.

[0329] When the emission luminance of light emitting materials are increased in the future, the light emitting device will be able to be applied to a front or rear type projector by expanding and projecting light containing image information having been output lenses or the like.

[0330] Cases are increasing in which the above-described electronic device displays information distributed via electronic communication lines such as the Internet and CATVs (cable TVs). Particularly increased are cases where moving picture information is displayed.

Since the response speed of the light emitting material is very high, the light emitting device is preferably used for moving picture display.

[0331] Since the light emitting device consumes the power in light emitting portions, information is desirably displayed so that the light emitting portions are reduced as much as possible. Thus, in the case where the light emitting device is used for a display portion of a mobile information terminal, particularly, a mobile telephone, an audio playback device, or the like, which primarily displays character information, it is preferable that the character information be formed in the light emitting portions with the non-light emitting portions being used as the background.

[0332] As described above, the application range of the present invention is very wide, so that the invention can be used for electronic device in all of fields. The electronic device according to this example may use the light emitting device with the structure according to any one of Embodiments 1 to 7 and Examples 1 to 4.

[0333] The present invention can reduce the effects of characteristic variations of the TFTs, and can offer a signal line drive circuit capable of supplying a desired signal current to the outside.

[0334] The present invention provides a light emitting device as described above in which a signal line drive circuit having a current source circuit is provided. Furthermore, the present invention provides a light emitting device capable of reducing the effects of the characteristic variations of TFTs that constitute both pixels and drive circuits and supplying a desired signal current I_{data} to light-emitting elements using the pixels with a circuit configuration in which the effects of the characteristic variations of TFTs are reduced.

Claims

1. A signal-line drive circuit comprising first and second current source circuits corresponding to respective plurality of signal lines; a shift register; and n (n is a natural number of one or more) video-signal constant current source s, **characterized in that**:

   each of the first and second current source circuits has a capacitance means and a supply means; wherein
   the capacitance means held in one of the first and second source circuits converts a current including a current supplied from each of the n video-signal constant current source s to voltage in accordance with a sampling pulse supplied from the shift register and a latch pulse supplied from the exterior; and the supply means held in the other supplies a current responsive to the converted voltage; and
   the values of the currents to be supplied from the n video-signal constant current source s are set at $2^0:2^1:\cdots:2^n$.

2. A signal-line drive circuit comptising (2 x n) current source circuits corresponding to respective plurality of signal lines; a shift register; and n (n is a natural number of one or more) video-signal constant current source s, **characterized in that**:

   the (2 × n) current source circuits includes a capacitance means for converting a current supplied from either one of the n video-signal constant currant source s to voltage in accordance with a sampling pulse supplied from the shift register and a latch pulse supplied from the exterior; and a supply means for supplying a current responsive to the converted voltage;
   a current is supplied to each of the plurality of signal lines from the n current source circuits selected from the (2 × n) current source circuits; and
   the values of the currents to be supplied from the n video-signal constant current source s are set at $2^0:2^1:\cdots:2^n$.

3. The signal-line drive circuit according to any one of Claims 1 and 2, **characterized in that**:

   when the drain and the gate of a transistor held in the supply means is short-circuited, the capacitance means holds a voltage generated between the gate and the source by the supplied current.

4. The signal-line drive circuit according to any one of Claims 1 and 2, **characterized in that**:

   the supply means comprises a transistor; a first switch for controlling the communication between the gate and the drain of the transistor; a second switch for controlling the communication between the video-Signal constant current source and the gate of the transistor; and a third switch for controlling the drain of the transistor and pixels.

5. The signal-line drive circuit according to any one of Claims 1 and 2, **characterized in that**:

   when the drains and the gates of both first and second transistors held in the supply means are short-circuited, the capacitance means holds a voltage generated between the gate and the source of the first or second transistor.

6. The signal-line drive circuit according to any one of Claims 1 and 2, **characterized in that**:

   the supply means comprises a current mirror

circuit including first and second transistors; a first switch for controlling the communication between the gates and the source of the first and second transistors; and a second switch for controlling the communication between the video-signal constant current source and the gates of the first and second transistors.

7. The signal-line drive circuit according to any one of Claims 1 and 2, **characterized in that**:

when the drain and the gate of one of first and second transistors held in the supply means are short-circuited, the capacitance means holds a voltage generated between the gate and the source by the supplied current.

8. The signal-line drive circuit according to any one of Claims 1 and 2, **characterized in that**:

the supply means comprises a current mirror circuit including first and second transistors;
a first switch for controlling the communication between the video-signal constant current source and the drain of the first transistor; and
a second switch for controlling the communication between the drain and the gate of the first transistor, the gate of the first transistor and the gate of the second transistor, the gates of the first and second transistors and either one of the video-signal constant current source s.

9. The signal-line drive circuit according to any one of Claims 6 to 8, **characterized in that**:

the values of the gate width/gate length of the first and second transistors are set to the same value.

10. The signal-line drive circuit according to any one of Claims 6 to 8, **characterized in that**:

the value of the gate width/gate length of the first transistor is set larger than the value of the gate width/gate length of the second transistor.

11. The signal-line drive circuit according to any one of Claims 1 and 2, **characterized in that**:

the supply means comprises a transistor; first and second switches for controlling the supply of the current to the capacitance means; and a third switch for controlling the communication between the gate and the drain of the transistor; wherein
the gate of the transistor is connected to the first switch; the source of the transistor is connected to the second switch; and the drain of the transistor is connected to the third switch.

12. The signal-line drive circuit according to any one of Claims 1 and 2, **characterized in that**:

the supply means comprises a current mirror circuit including m transistors; wherein
the values of the gate width/gate length of the m transistor are set to a proportion of $2^0:2^1:\cdots:2^m$; and
the drain currents of the m transistors are set to a proportion of $2^0:2^1:\cdots:2^m$.

13. The signal-line drive circuit according to any one of Claims 1 and 2, **characterized in that**:

transistors constituting the supply means operate in a saturated area.

14. The signal-line drive circuit according to any one of Claims 1 and 2, **characterized in that**:

active layers of the transistors constituting the current source circuit are formed of polysilicon.

15. A light emitting device **characterized by** comprising the signal-line drive circuit of any one of Claims 1 and 2 and a pixel section having a plurality of pixels each including a light-emitting element arranged in matrix.

Amended claims under Art. 19.1 PCT

1. (Amended) A signal-line drive circuit comprising:

first and second current source circuits corresponding to respective plural signal lines;
a shift register,

wherein each of the first and second current source circuits comprises a capacitive element,
wherein one of the first and second source circuits converts a current obtained by adding currents supplied from n pieces of video-signal current sources to a voltage in accordance with a sampling pulse supplied from the shift register and a latch pulse supplied from the exterior and holds the voltage by the capacitive element,
wherein n is a natural number,
wherein the other of the first and second source circuits supplies a current corresponding to the voltage to a corresponding signal line, and
wherein the values of the currents to be supplied from the n pieces of video-signal current sources are set at $2^0:2^1:\cdots:2^{n-1}$.

2. (Amended) A signal-line drive circuit comprising:

(2 × n) pieces of current source circuits corresponding to respective plural signal lines;
a shift register,

wherein n is a natural number,
wherein each of the (2 × n) pieces of current source circuits comprises a capacitive element,
wherein two of the (2 × n) pieces of current source circuits corresponds to each of n pieces of video-signal current sources,
wherein one of the two current source circuits converts a current supplied from the corresponding video signal current source to a voltage in accordance with a sampling pulse supplied from the shift register and a latch pulse supplied from an exterior and holds the voltage by the capacitive element, and
wherein the other of the two current source circuits supplies a current corresponding to the voltage to a corresponding signal line, and
wherein the values of the currents to be supplied from the n pieces of video-signal current sources are set at $2^0:2^1:\cdots:2^{n-1}$.

3. (Amended) The signal-line drive circuit according to any one of Claims 1 and 2,
wherein at least one of the current source circuits further comprises a transistor,
wherein when a drain and a gate of the transistor is short-circuited, by a charge accumulated in the capacitive element, a voltage generated between the gate and a source of the transistor is held.

4. (Amended) The signal-line drive circuit according to any one of Claims 1 and 2,
wherein at least one of the current source circuits further comprises :

a transistor;
a first switch for controlling the communication between a gate and a drain of the transistor;
a second switch for controlling the communication between the video-signal current source and the gate of the transistor; and
a third switch for controlling a communication of the drain of the transistor and a pixel.

5. (Amended) The signal-line drive circuit according to any one of Claims 1 and 2,
wherein at least one of the current source circuits further comprising first and second transistors,
wherein when drains and gates of both the first and second transistors are short-circuited, by a charge accumulated in the capacitive element due to the supplied current, a voltage generated between the gate and the source of one of the first and second transistors.

6. (Amended) The signal-line drive circuit according to any one of Claims 1 and 2,
wherein at least one of the current source circuits further comprises:

a current mirror circuit comprising first and second transistors; a first switch for controlling a communication between a gate and a drain of the first transistor; and
a second switch for controlling a communication between the video-signal current source and one of a source and the drain of the first transistor.

7. (amended) The signal-line drive circuit according to any one of Claims 1 and 2,
wherein at least one of the current source circuits further comprises a first and second transistors,
wherein when a drain and a gate of the first transistor are short-circuited, by a charge accumulated in the capacitive element due to the supplied current, a voltage generated between the gate and a source is held.

8. (Amended) The signal-line drive circuit according to any one of Claims 1 and 2,
wherein at least one of the current source circuits further comprises:

a current mirror circuit comprising first and second transistors;
a first switch for controlling a communication between the video-signal current source and one of a source and a drain of the first transistor; and
a second switch for controlling one of communications between the drain and a gate of the first transistor, between the gate of the first transistor and a gate of the second transistor, and among the gates of the first and second transistors and the video-signal current source.

9. (Amended) The signal-line drive circuit according to any one of Claims 6 to 8,
wherein the values of the gate width/gate length of the first and second transistors are set to the same value.

10. (Amended) The signal-line drive circuit according to any one of Claims 6 to 8,
wherein the value of the gate width/gate length of the first transistor is set larger than the value of the gate width/gate length of the second transistor.

11. (Amended) The signal-line drive circuit according to any one of Claims 1 and 2,

wherein at least one of the current source circuits further comprises:

a transistor;
first and second switches for controlling a supply of a current to the capacitive element; and
a third switch for controlling a communication between a gate and a drain of the transistor,

wherein the gate of the transistor is connected to the third switch,
wherein a source of the transistor is connected to the first switch, and
wherein the drain of the transistor is connected to the second switch.

12. (Amended) The signal-line drive circuit according to any one of Claims 1 and 2,
wherein at least one of the current source circuits comprises a current mirror circuit comprising m pieces of transistors,
wherein the values of gate width/gate length of the m pieces of transistors are set to a proportion of $2^0:2^1:\cdots:2^{m-1}$, and
wherein the drain currents of the m pieces of transistors are set to a proportion of $2^0:2^1:\cdots:2^{m-1}$.

13. (Amended) The signal-line drive circuit according to any one of Claims 1 and 2,
wherein at least one of the transistors constituting the current source circuits operates in a saturated area.

14. (Amended) The signal-line drive circuit according to any one of Claims 1 and 2,
wherein an active layer of at least one of the transistors constituting the current source circuit comprises polysilicon.

15. (Amended) A light emitting device comprising the signal-line drive circuit of any one of Claims 1 and 2 and a pixel section having a plurality of pixels, wherein each of the pixels comprises a light-emitting element arranged in matrix.

Fig. 1

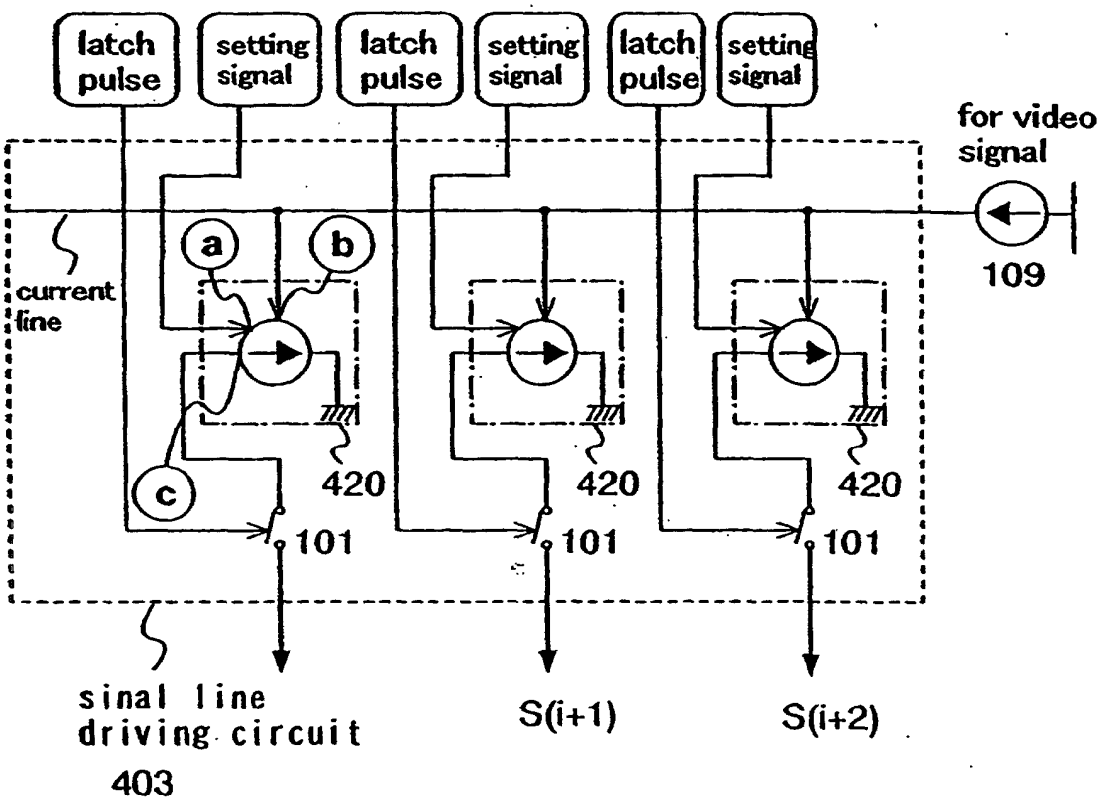

latch pulse
setting signal
latch pulse
setting signal
latch pulse
setting signal
for video signal
109
current line
a
b
c
420
420
420
101
101
101
sinal line driving circuit
403
S(i+1)
S(i+2)

Fig. 2

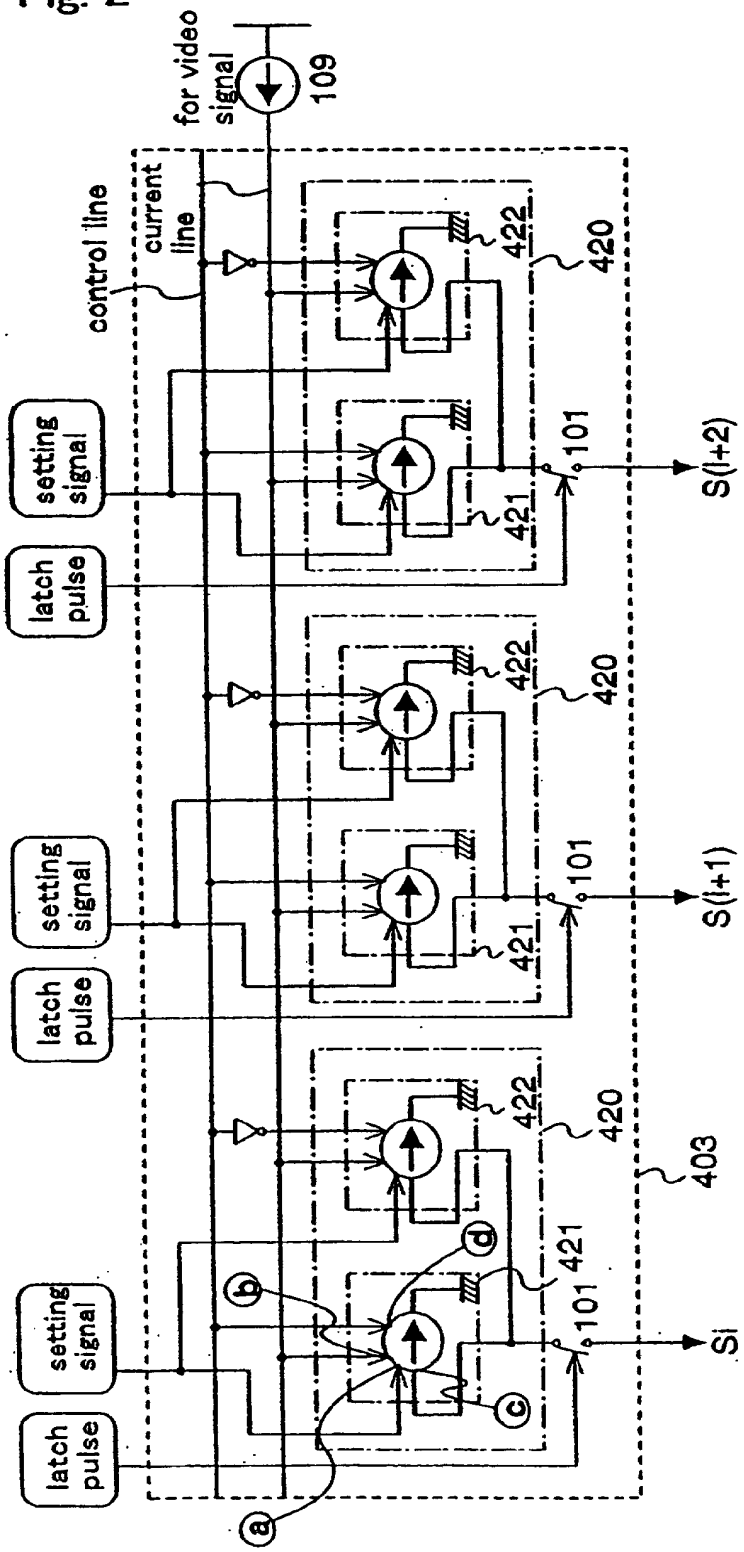

for video signal
109
control line
current line
422
420
setting signal
latch pulse
421
101
S(i+2)
S(i+1)
Si
403
a
b
c
d

Fig. 3A

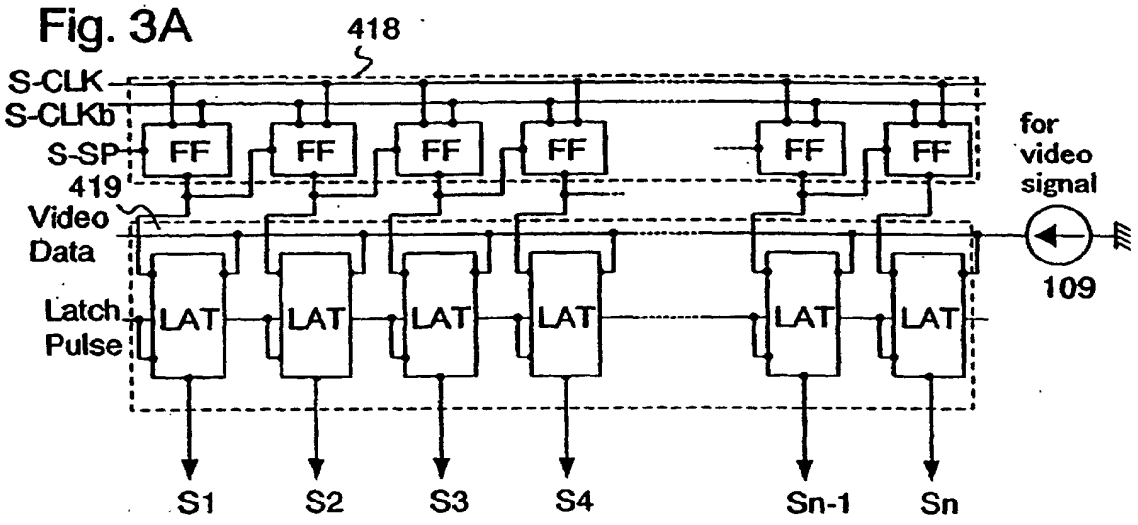

418
S-CLK
S-CLKb
S-SP
FF
419
Video
Data
Latch
Pulse
LAT
for
video
signal
109
S1
S2
S3
S4
Sn-1
Sn

Fig. 3B

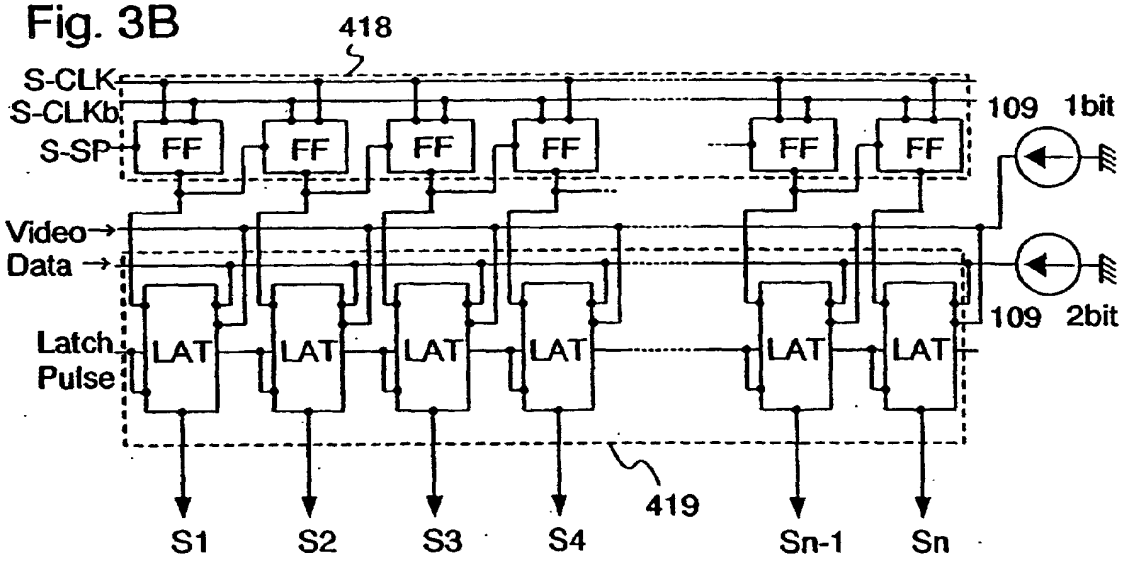

418
S-CLK
S-CLKb
S-SP
FF
Video
Data
Latch
Pulse
LAT
109
1bit
109
2bit
419
S1
S2
S3
S4
Sn-1
Sn

Fig. 4

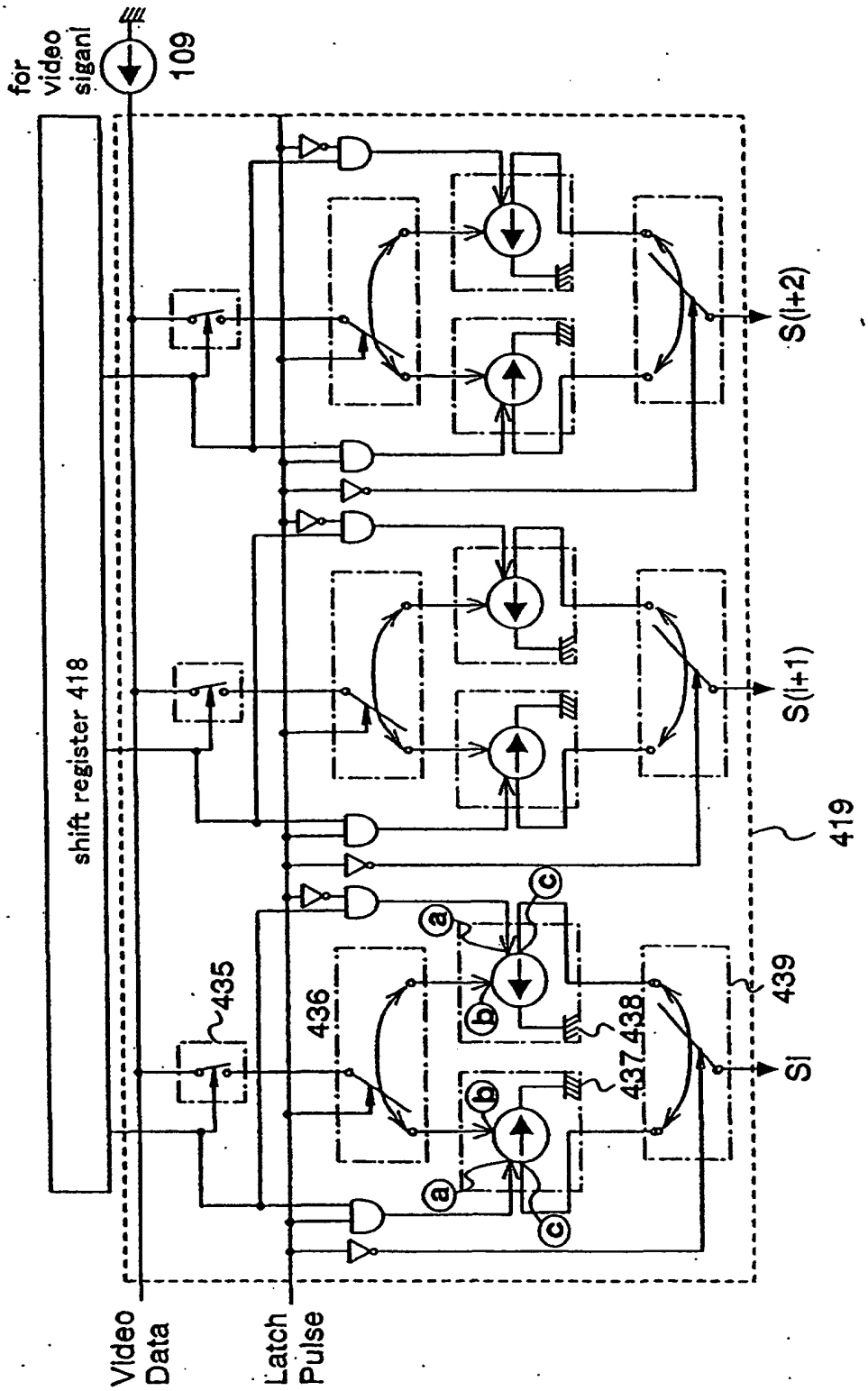

for video signal
109
shift register 418
S(i+2)
S(i+1)
419
435
436
437
438
439
SI
Video Data
Latch Pulse
a
b
c

Fig. 5

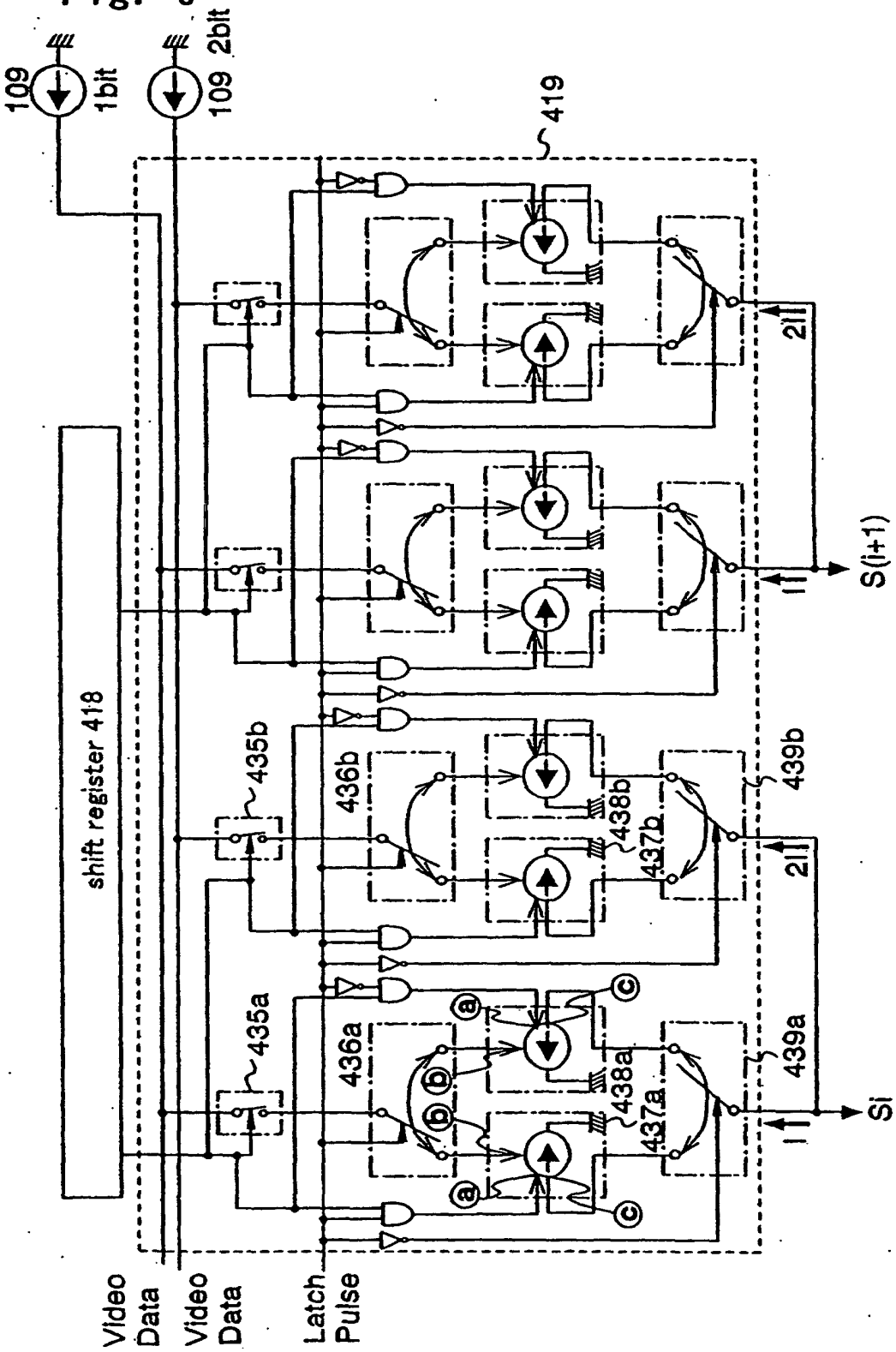

109
1bit
109
2bit
419
shift register 418
435b
436b
438b
437b
439b
435a
436a
438a
437a
439a
2II
S(i+1)
Si
Video Data
Video Data
Latch Pulse

Fig. 6A

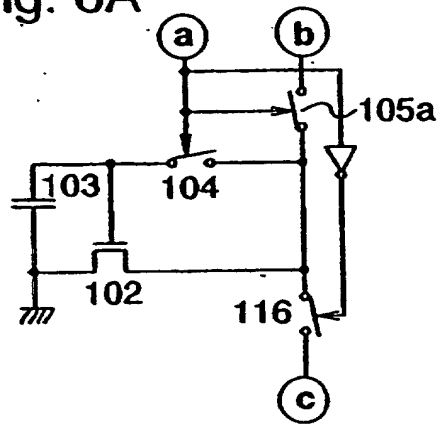


Fig. 6B

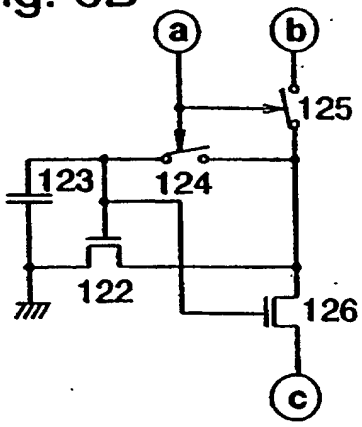


Fig. 6C

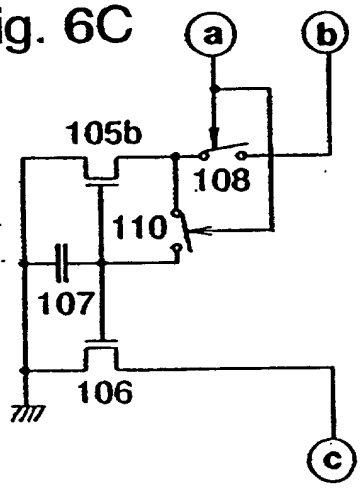


Fig. 6D

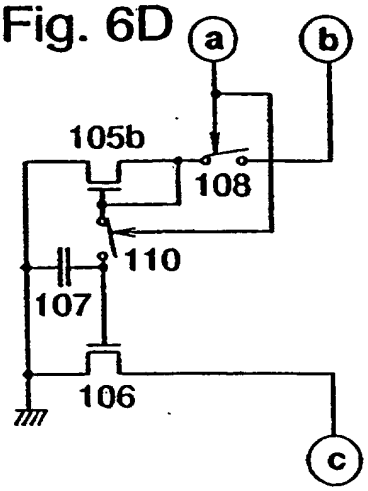


Fig. 6E

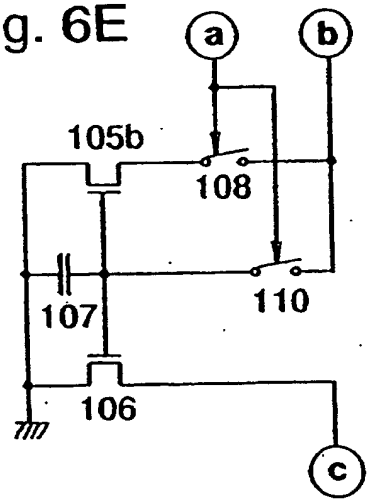


Fig. 7A

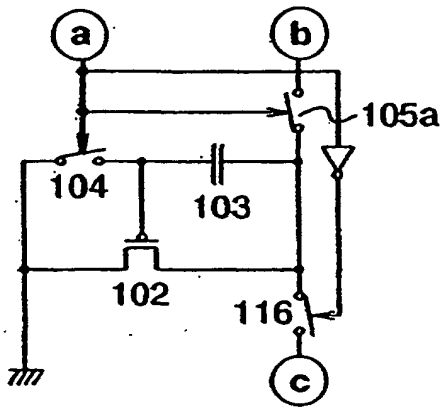


Fig. 7B

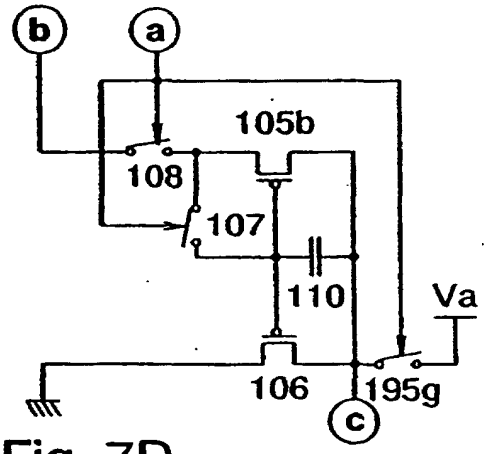


Fig. 7C

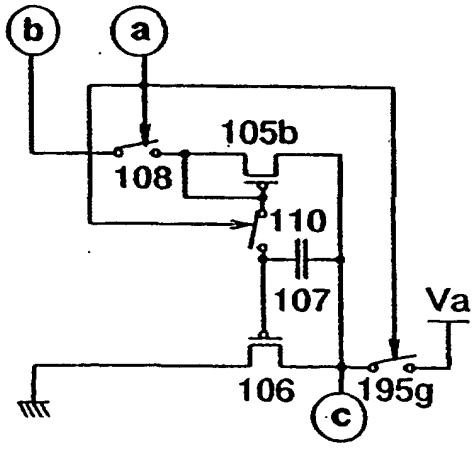


Fig. 7D

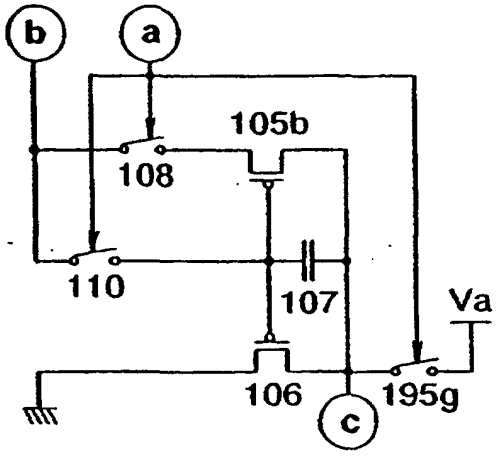


Fig. 8A

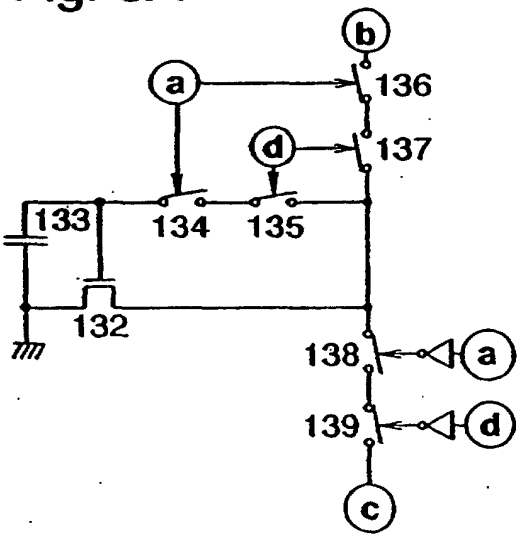

b
a
136
d
137
133
134
135
132
138
a
139
d
c

Fig. 8B

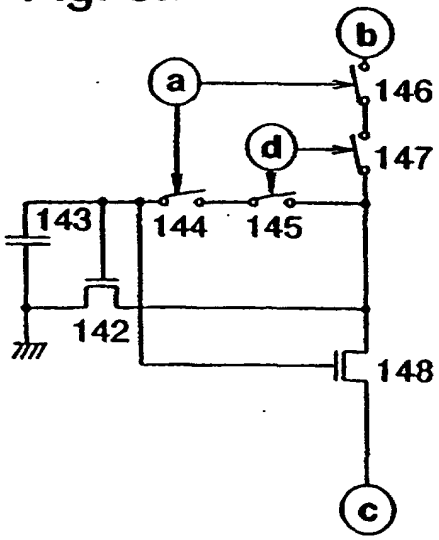

b
a
146
d
147
143
144
145
142
148
c

Fig. 9

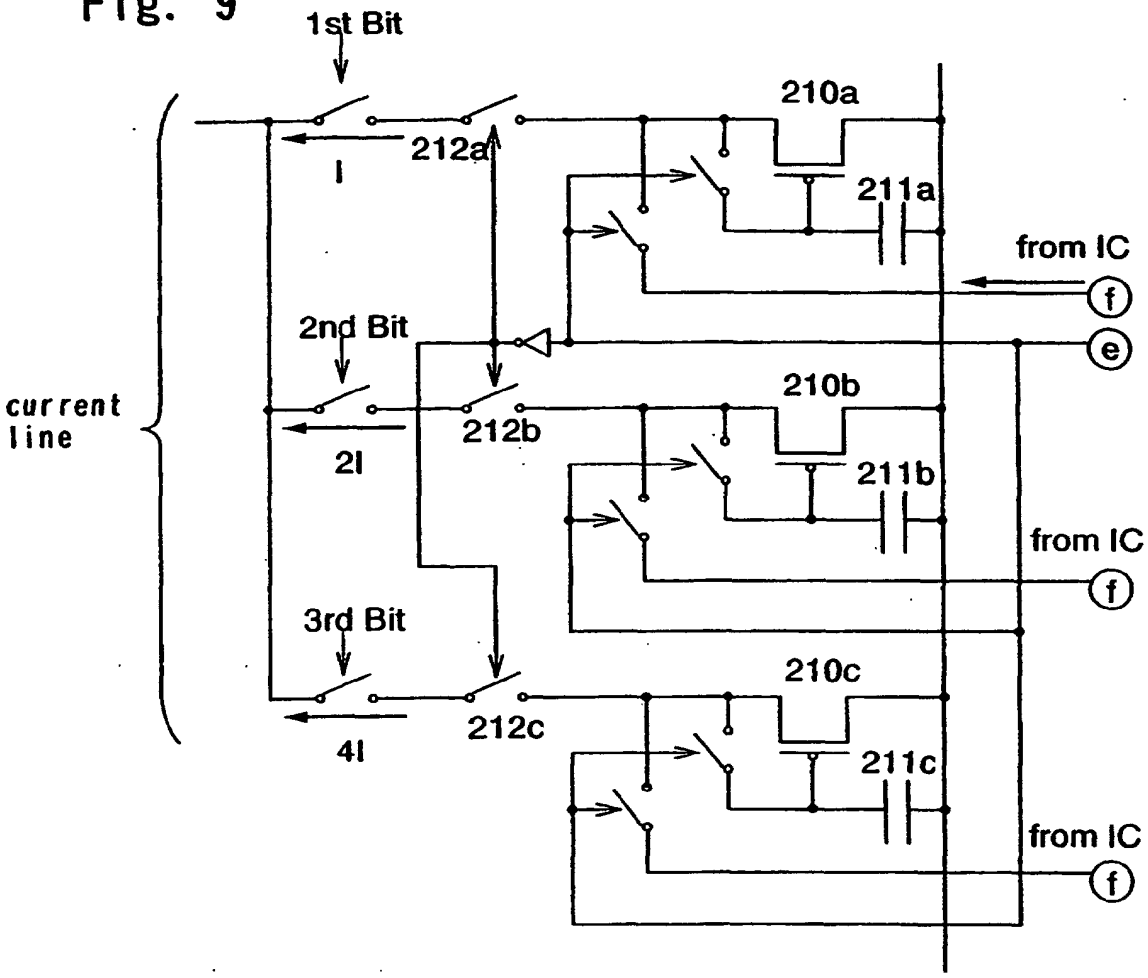

1st Bit
210a
212a
I
211a
from IC
f
2nd Bit
e
current line
210b
212b
2I
211b
from IC
f
3rd Bit
210c
212c
4I
211c
from IC
f

Fig. 10

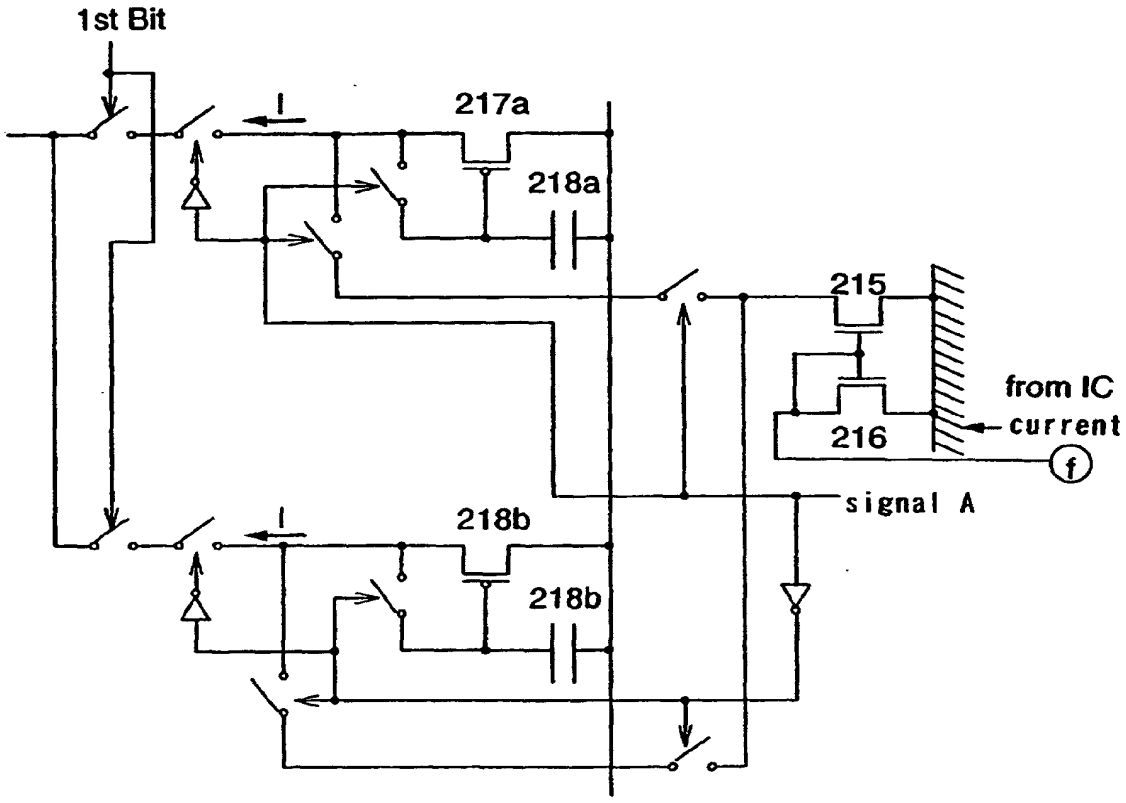

1st Bit
I
217a
218a
215
from IC
current
216
f
signal A
I
218b
218b

Fig. 11A

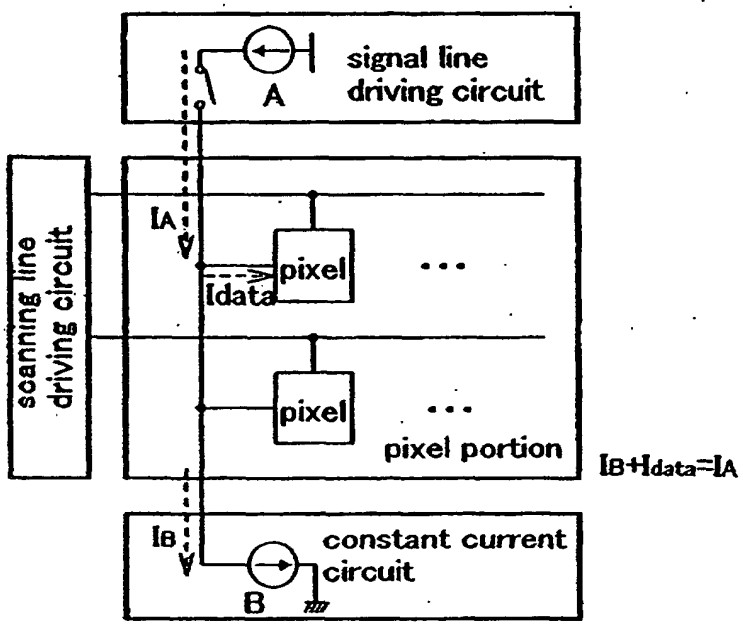


Fig. 11B

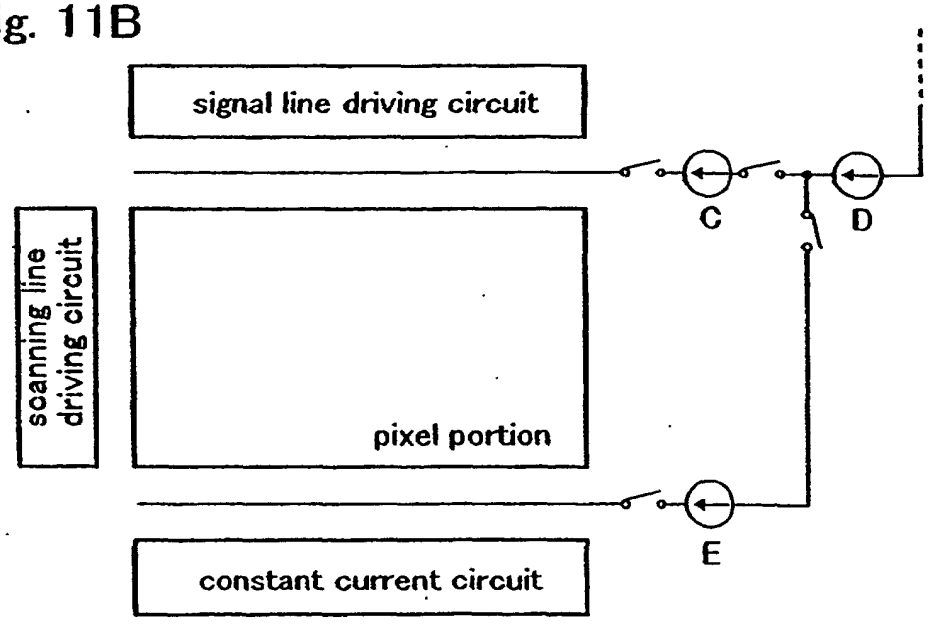


Fig. 12A

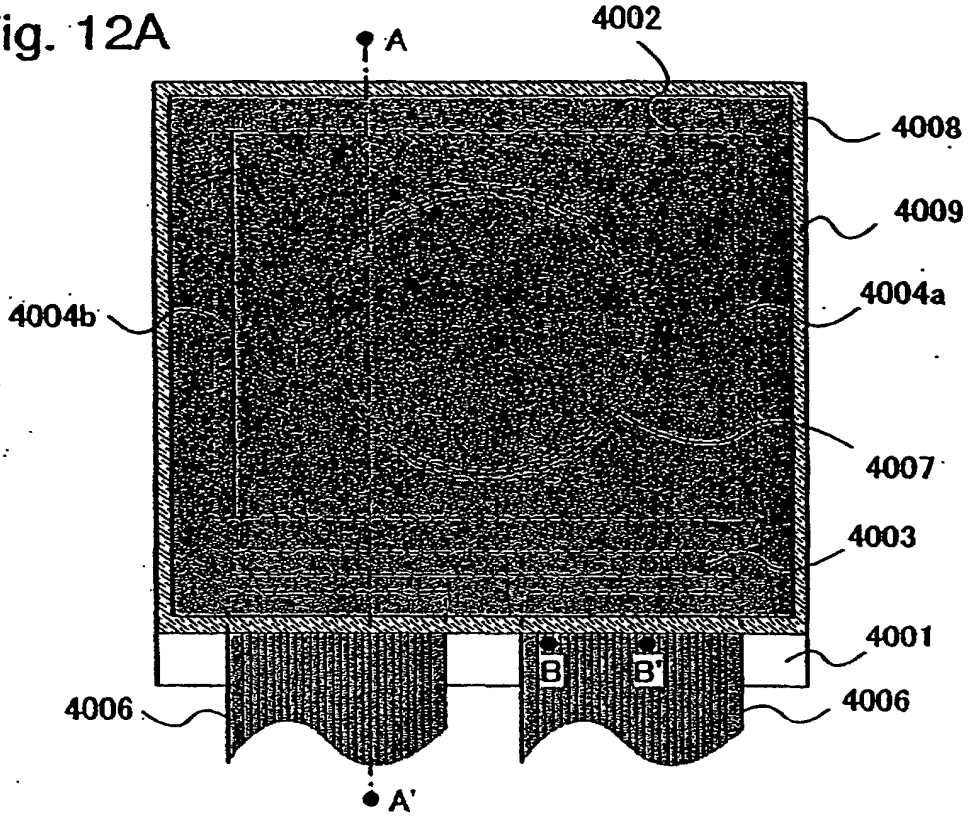


Fig. 12B

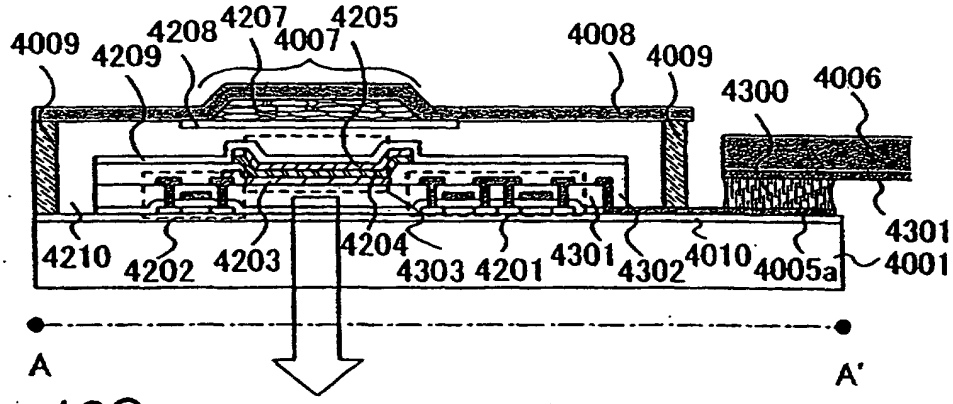


Fig. 12C

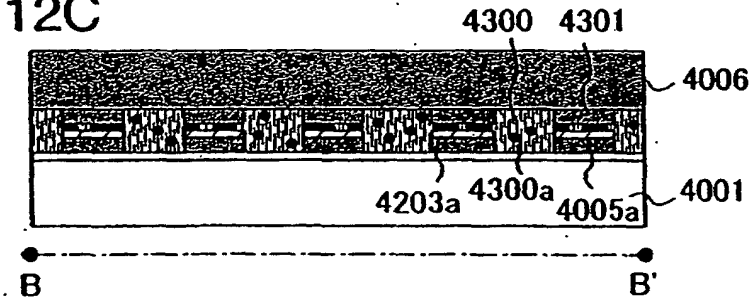


Fig. 13A

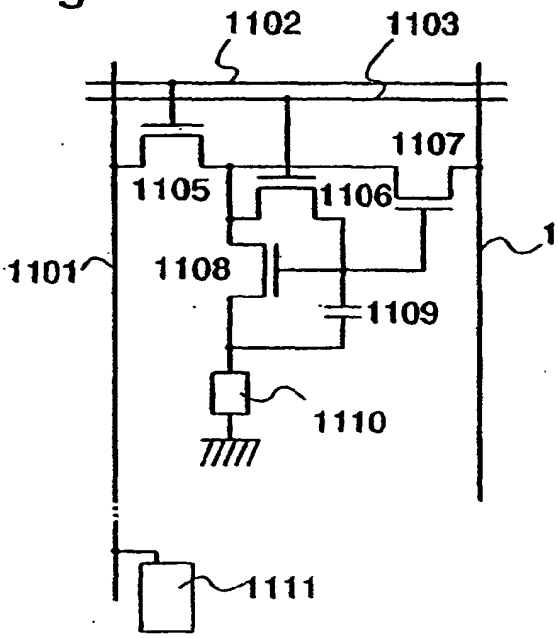


Fig. 13B

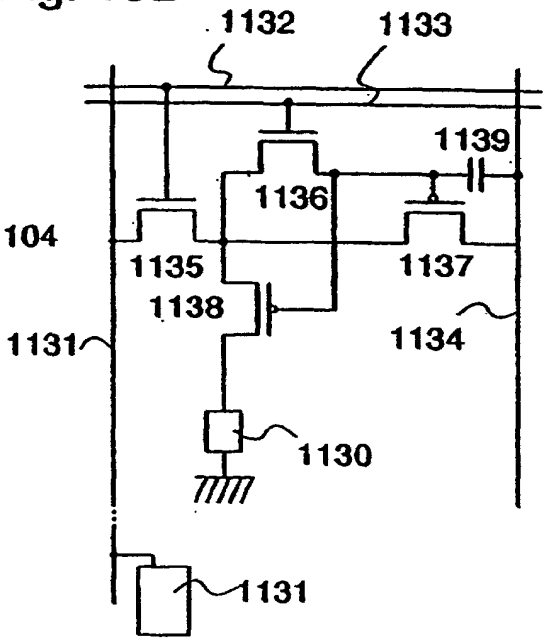


Fig. 13C

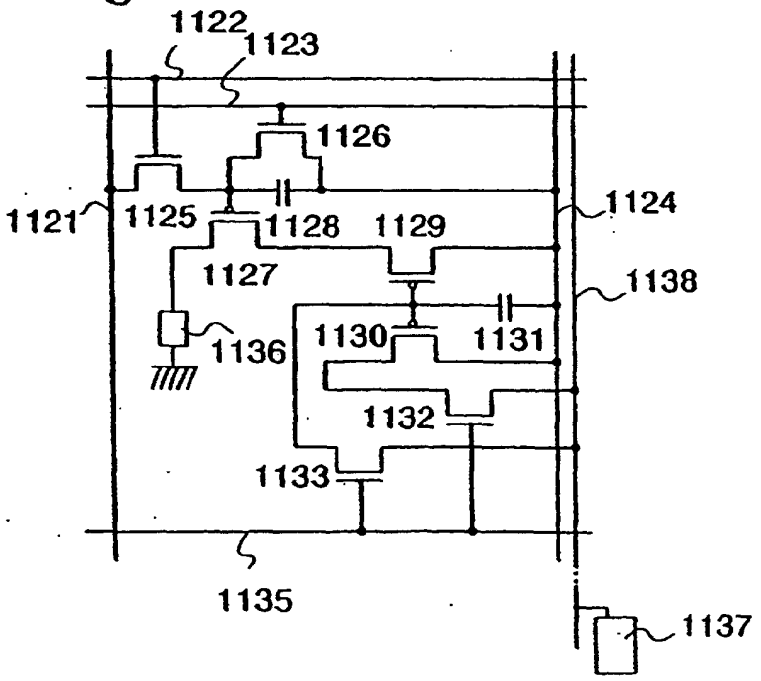


Fig. 14A

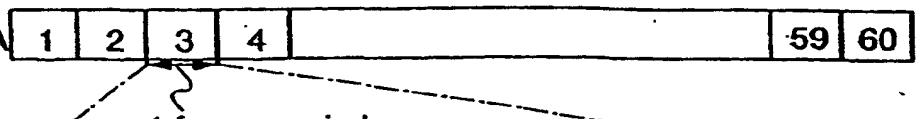


Fig. 14B

Fig. 14C

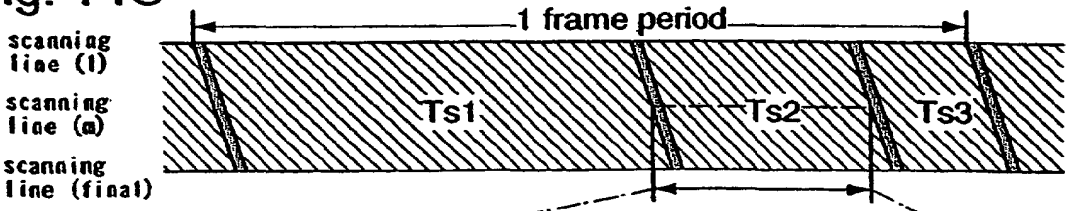


Fig. 14D

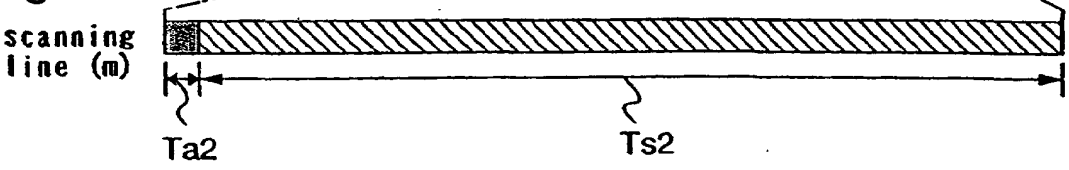


Fig. 15A

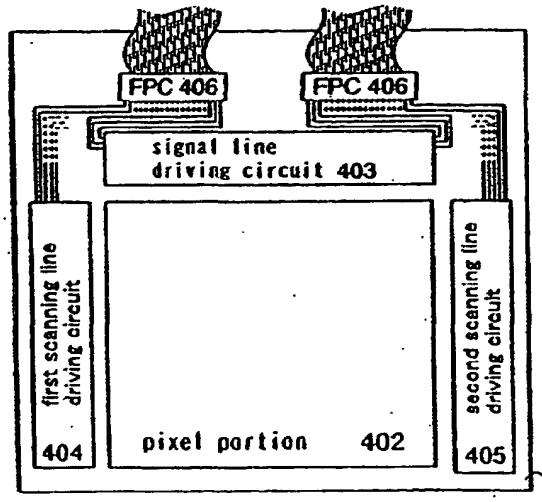


Fig. 15B

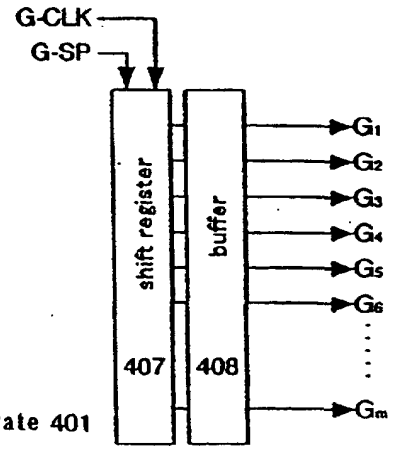


Fig. 16A

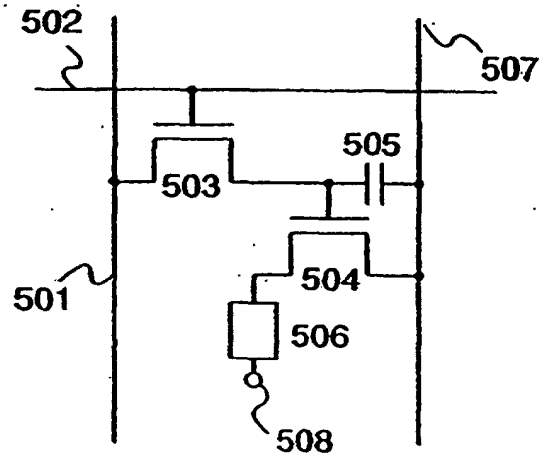


Fig. 16B

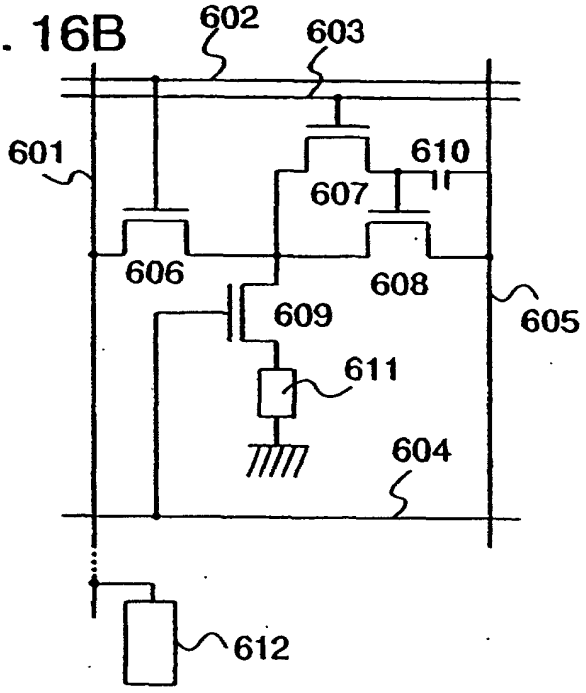


Fig. 17A signal input time

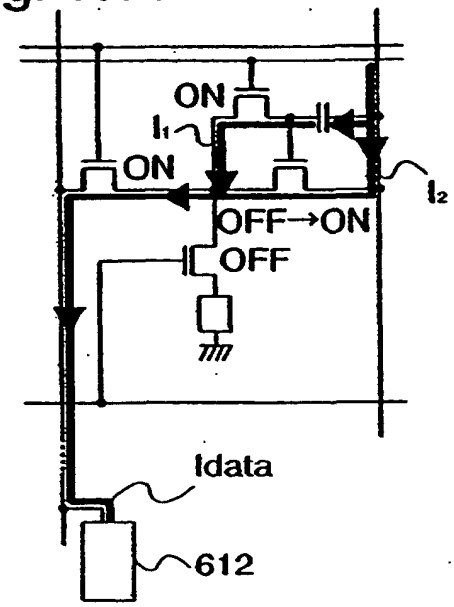


Fig. 17B signal input complete time

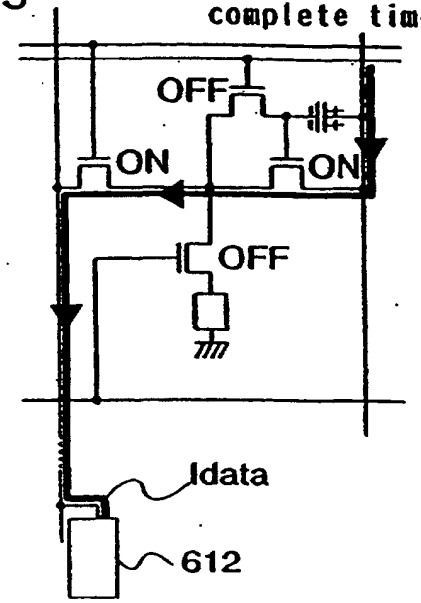


Fig. 17C light emitting time

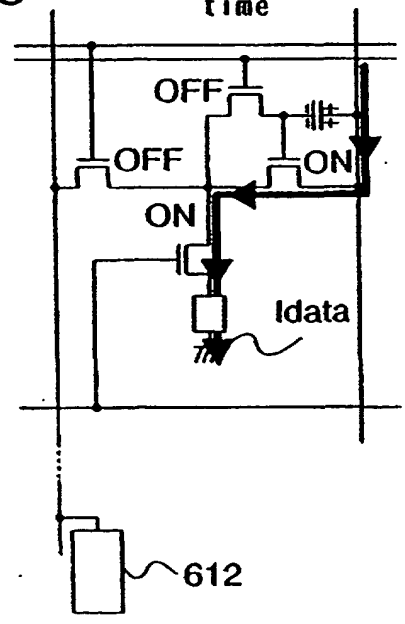


Fig. 17D

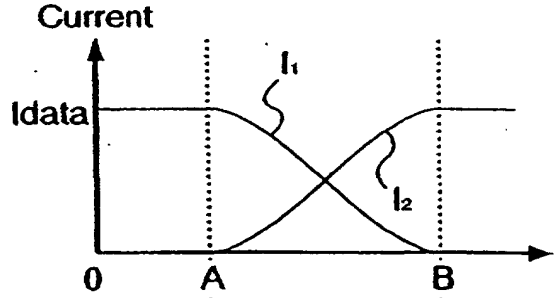


Fig. 17E

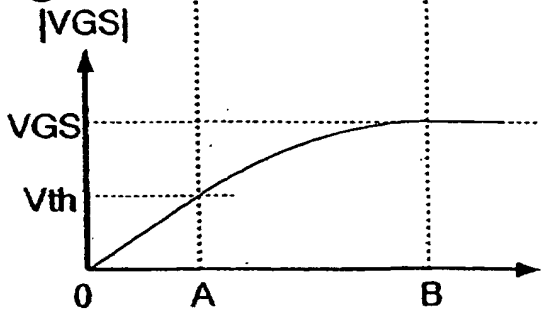


Fig. 18A

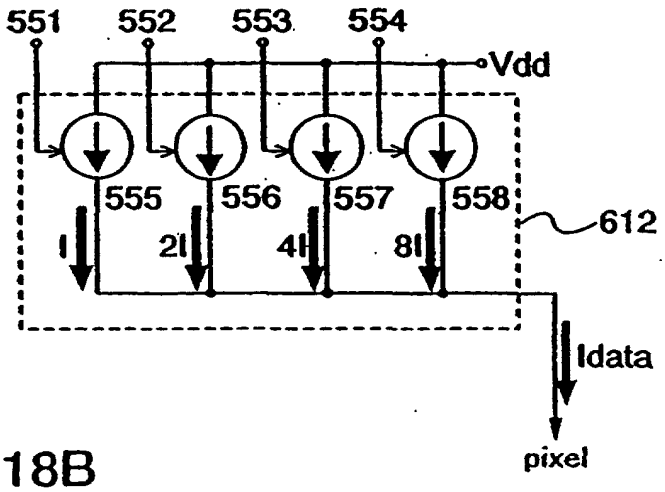


Fig. 18B

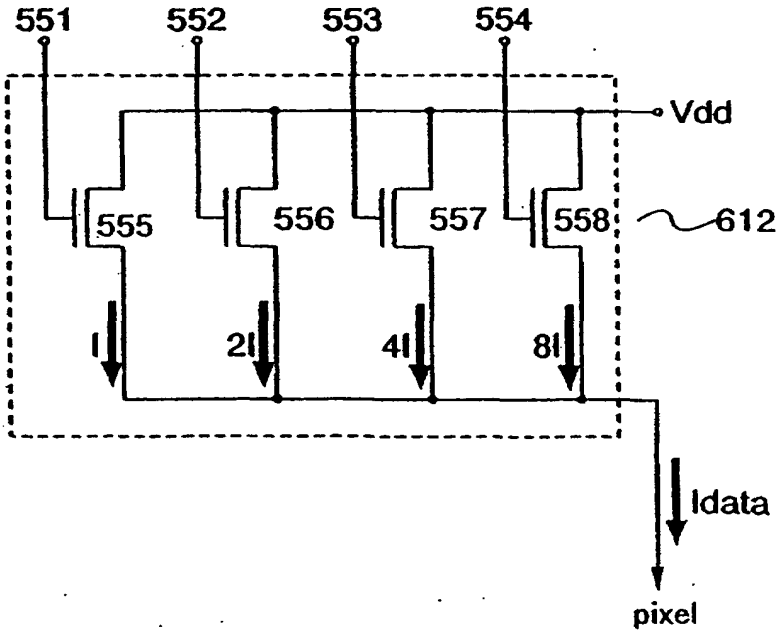


Fig. 19A

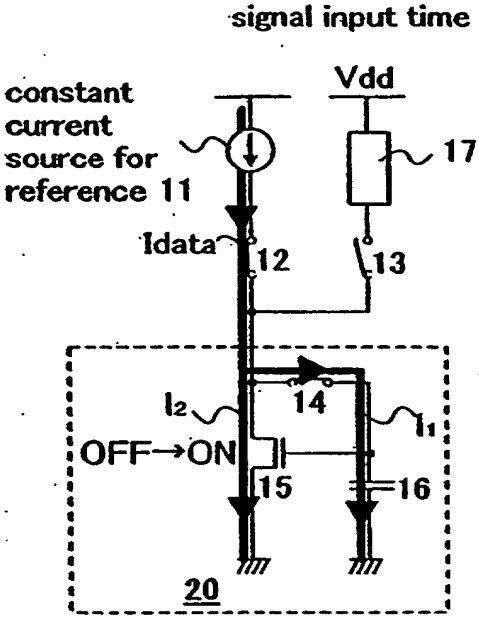


Fig. 19B

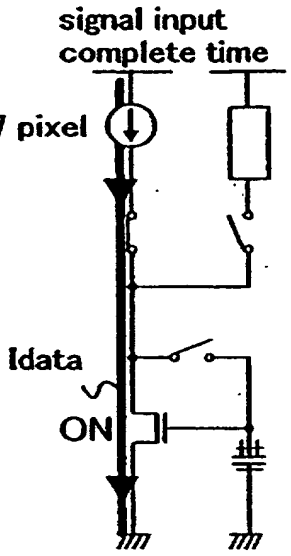


Fig. 19C

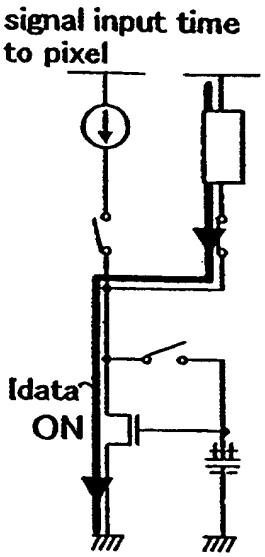


Fig. 19D

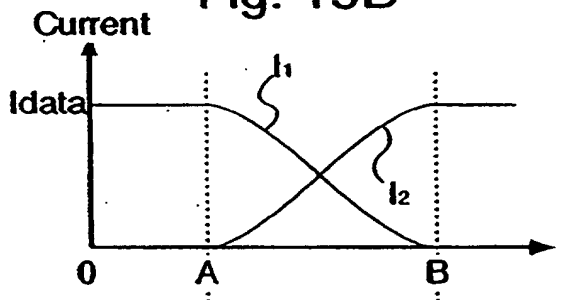


Fig. 19E

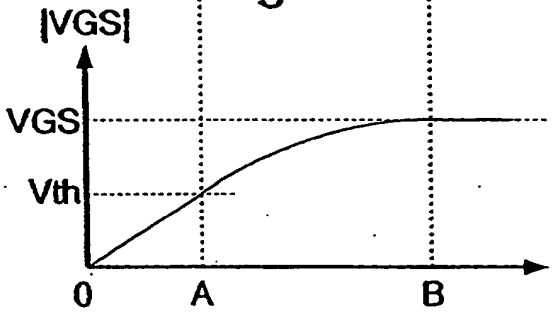


Fig. 19F

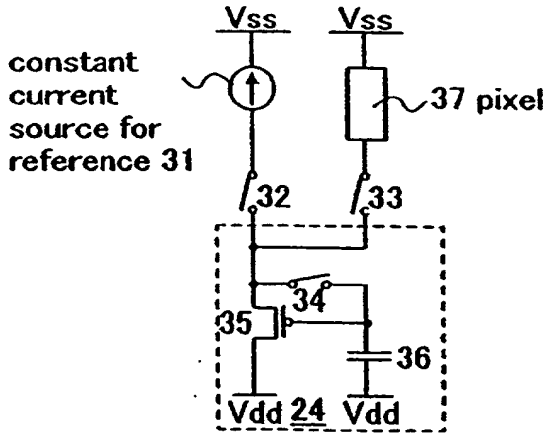


Fig. 20A signal input time

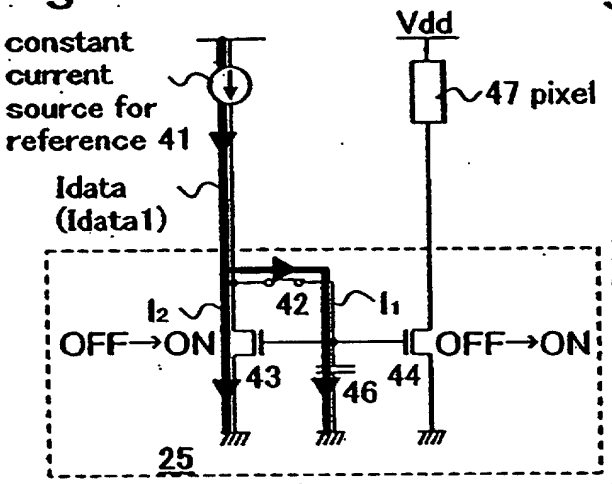


Fig. 20B signal input complete time

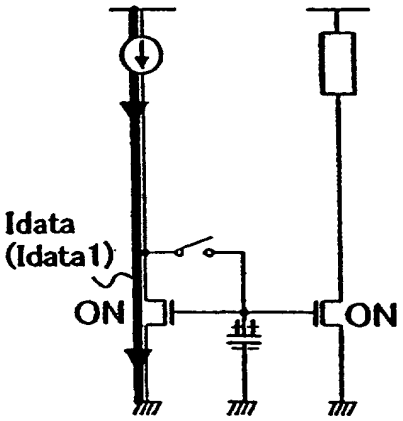


Fig. 20C signal input time to pixel

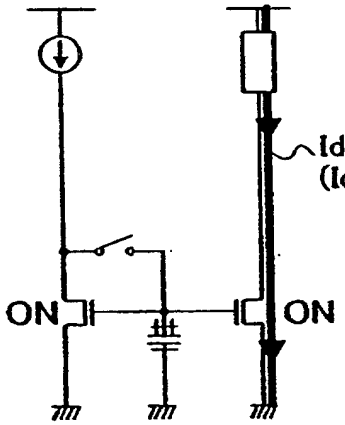


Fig. 20D

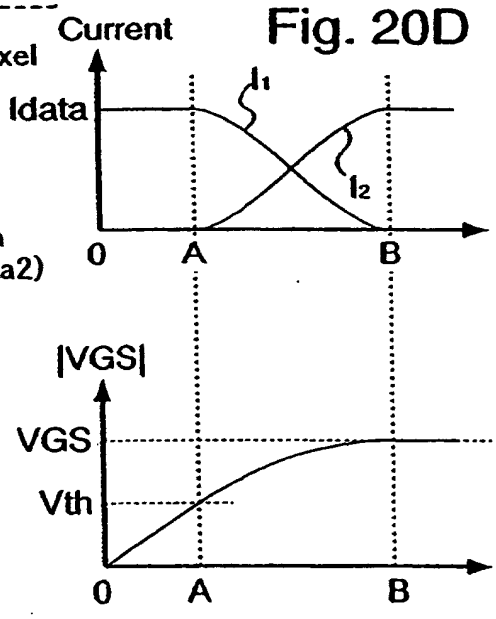


Fig. 20E

Fig. 21

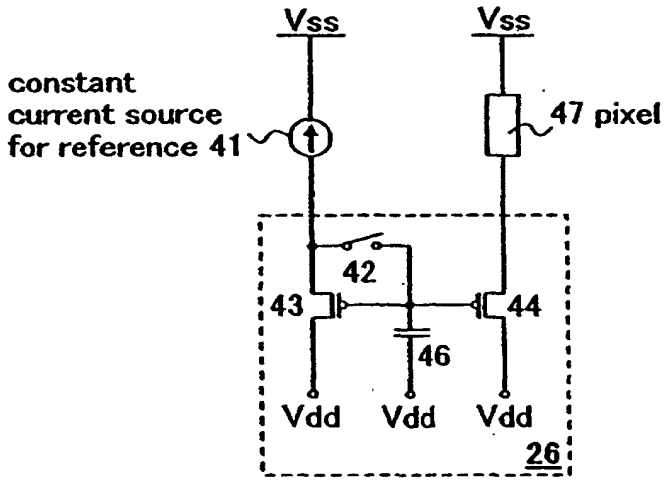

Vss
Vss
constant
current source
for reference 41
47 pixel
42
43
44
46
Vdd
Vdd
Vdd
26

Fig. 22A

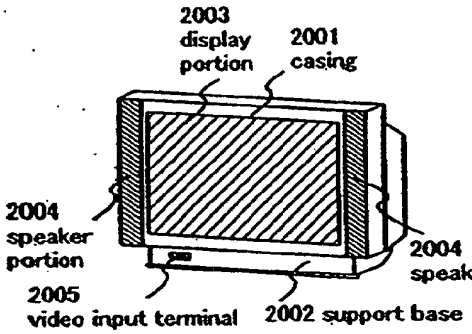


Fig. 22B

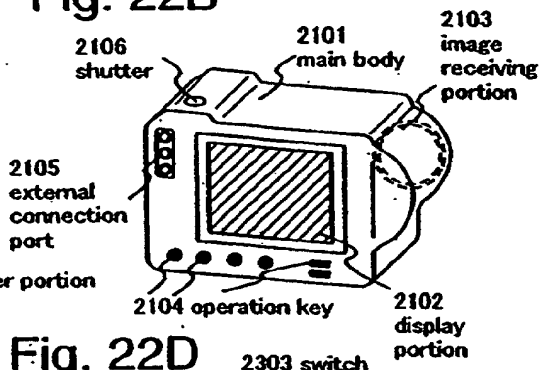


Fig. 22C

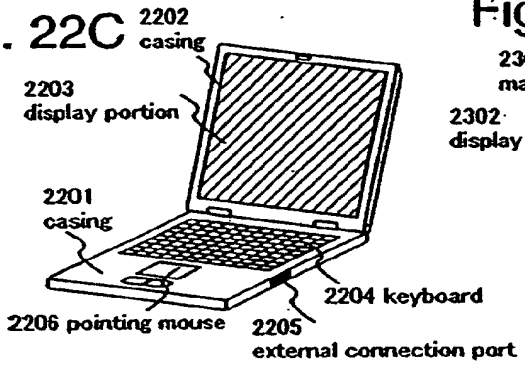


Fig. 22D

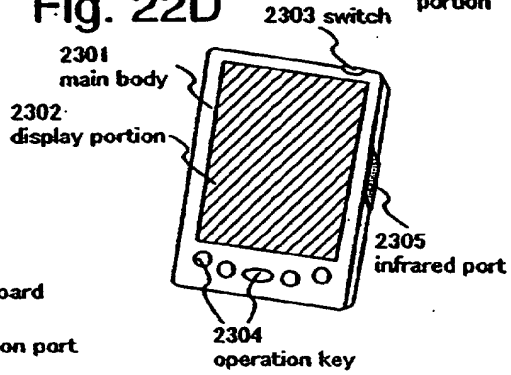


Fig. 22E

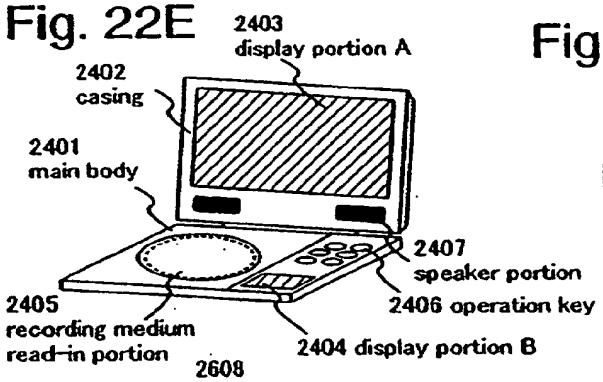


Fig. 22F

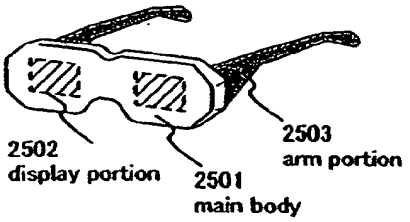


Fig. 22G

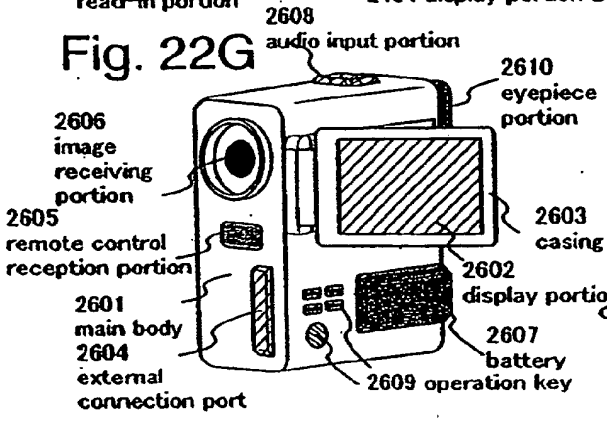


Fig. 22H

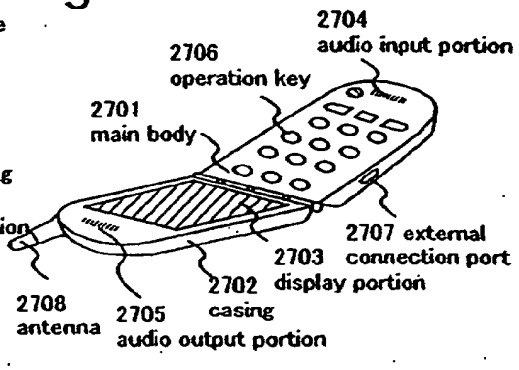


Fig. 23

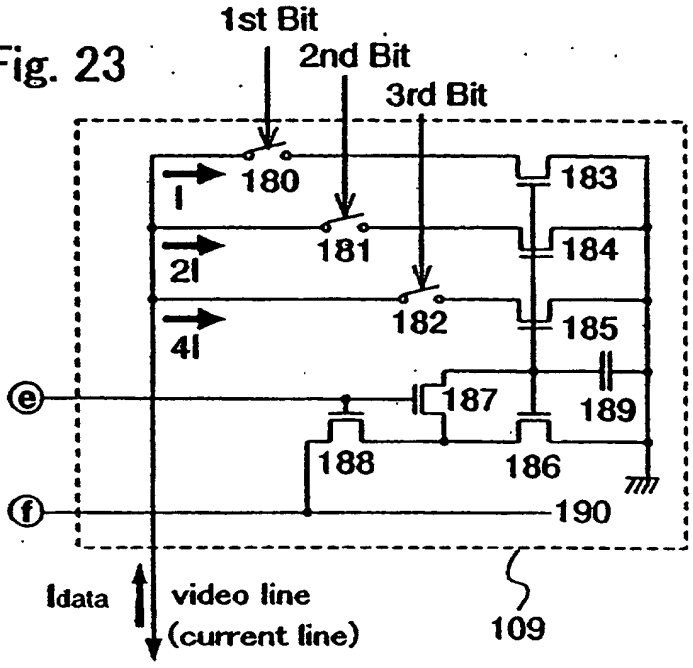

1st Bit
2nd Bit
3rd Bit
180
181
182
183
184
185
187
188
189
186
190
I
2I
4I
e
f
Idata
video line
(current line)
109

Fig. 24

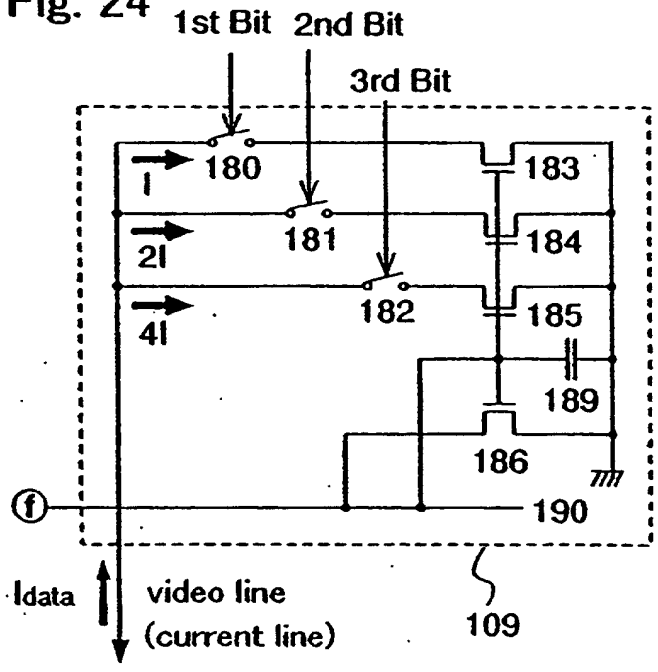

1st Bit
2nd Bit
3rd Bit
180
181
182
183
184
185
189
186
190
I
2I
4I
f
Idata
video line
(current line)
109

Fig. 25

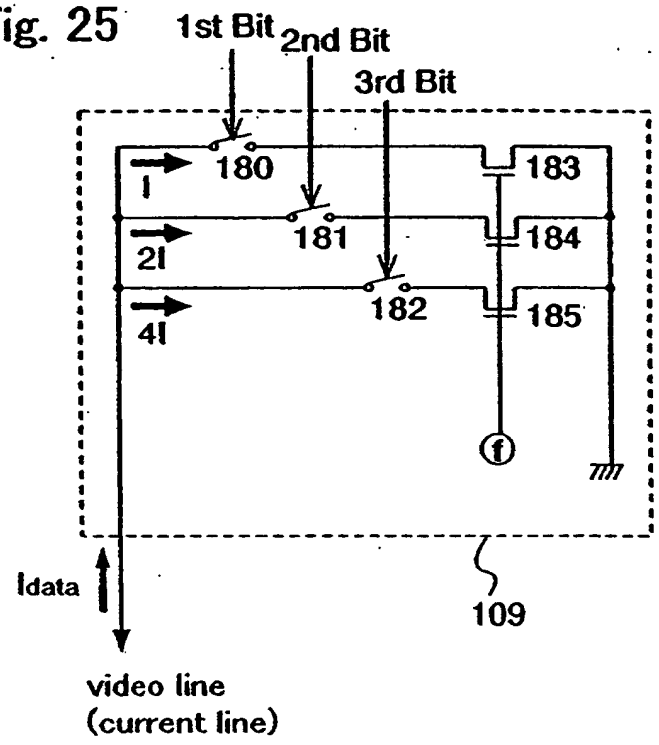

1st Bit
2nd Bit
3rd Bit
180
181
182
183
184
185
I
2I
4I
f
Idata
109
video line
(current line)

Fig. 26

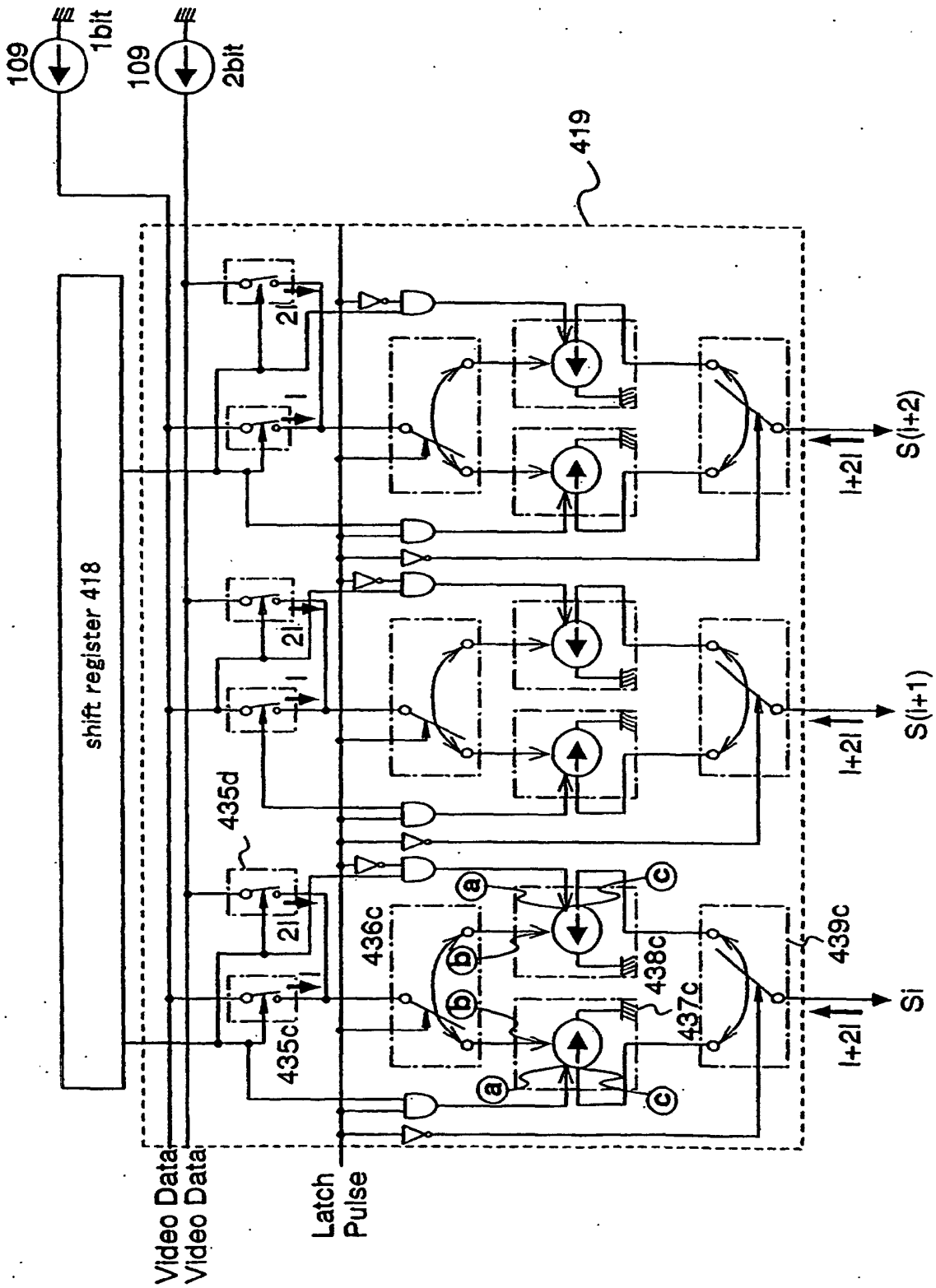

109
1bit
109
2bit
419
shift register 418
2I
I
I+2I
S(i+2)
S(i+1)
435d
436c
438c
437c
439c
435c
Si
Video Data
Video Data
Latch Pulse

Fig. 27A1

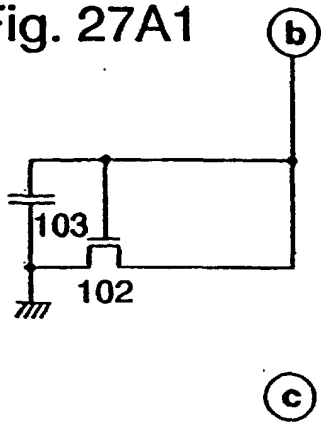


Fig. 27A2

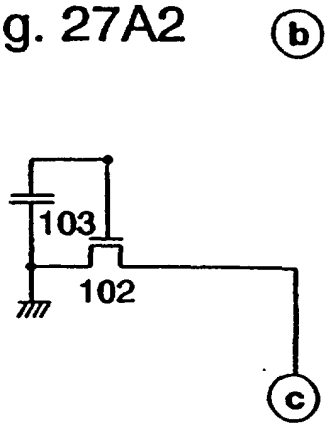


Fig. 27B1

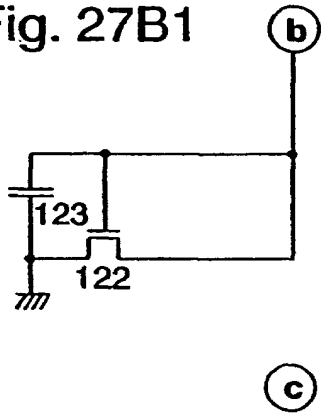


Fig. 27B2

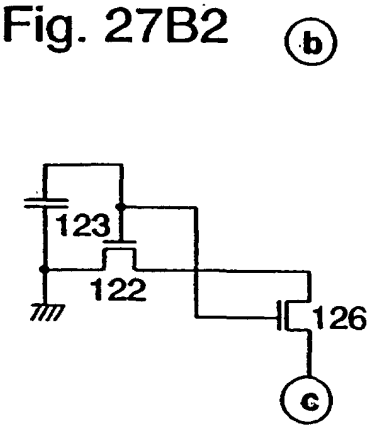


Fig. 27C1

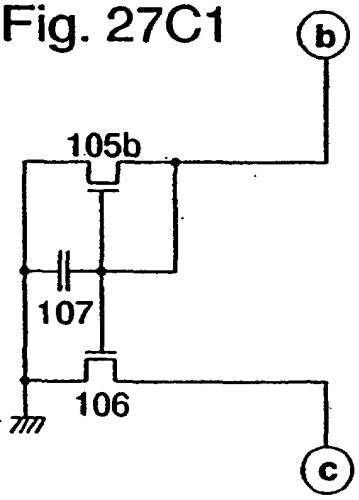


Fig. 27C2

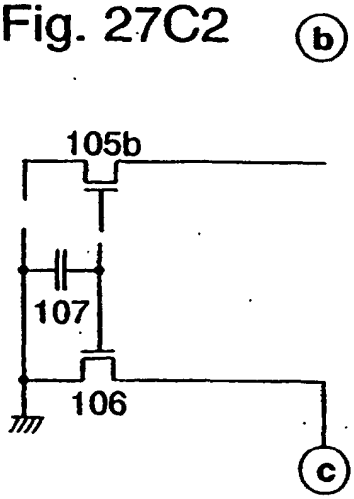


Fig. 28A

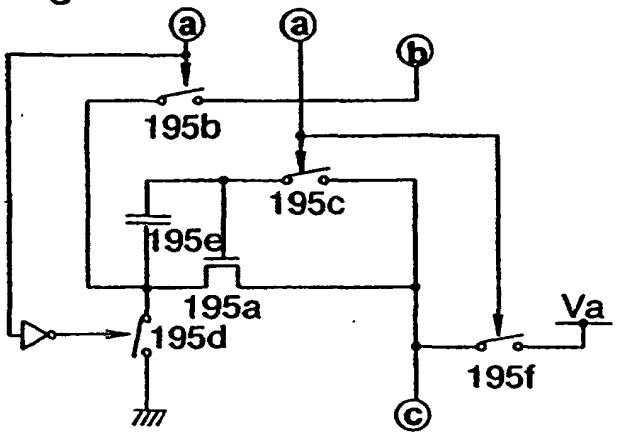


Fig. 28B1

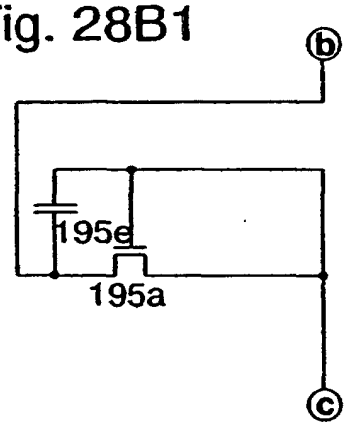


Fig. 28B2

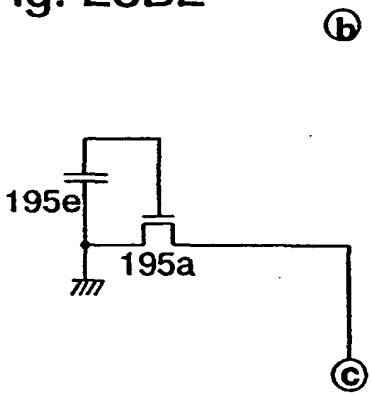


Fig. 28C1

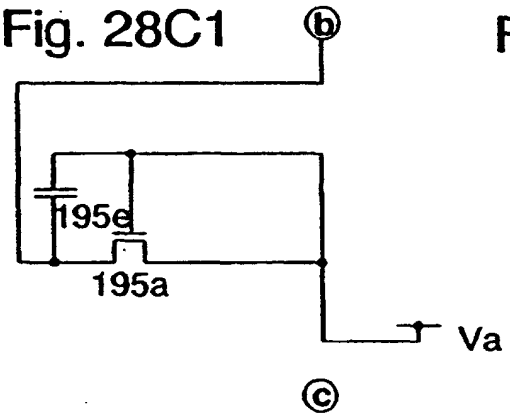


Fig. 28C2

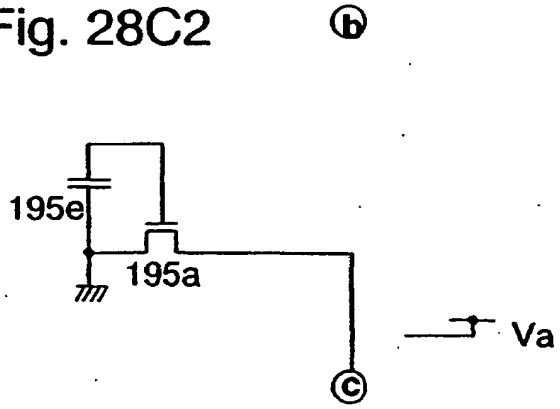


Fig. 29A

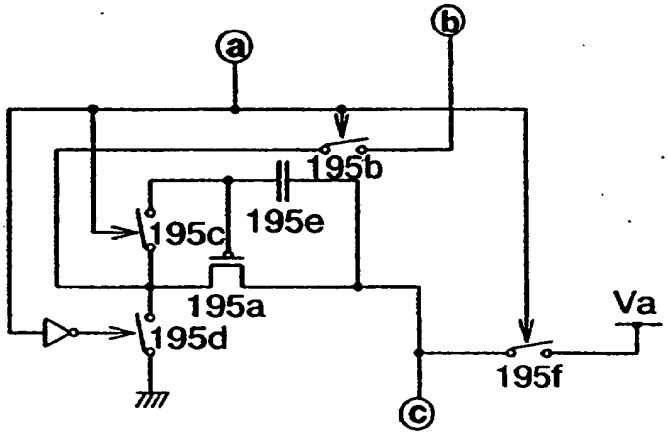


Fig. 29B

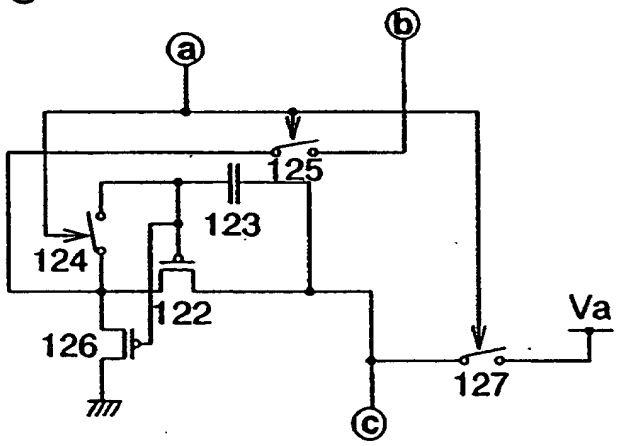


Fig. 30A1

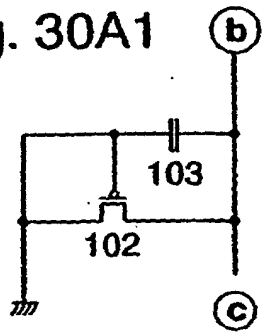


Fig. 30A2

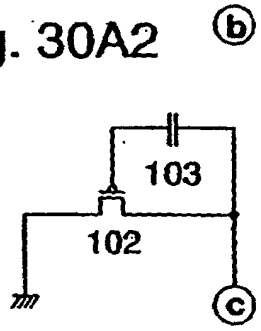


Fig. 30B1

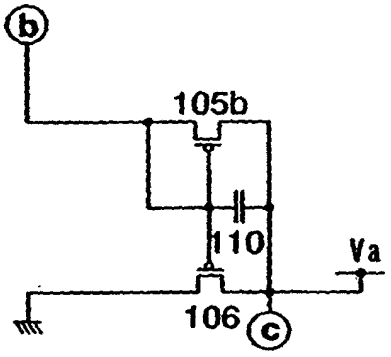


Fig. 30B2

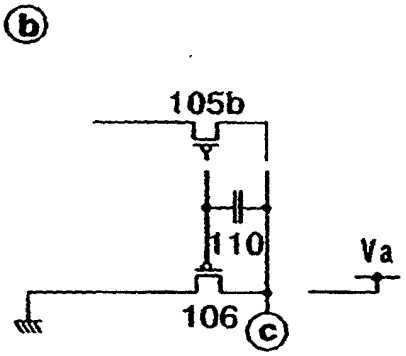


Fig. 30C1

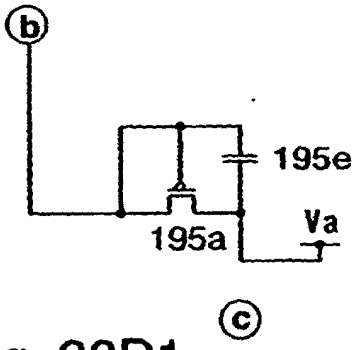


Fig. 30C2

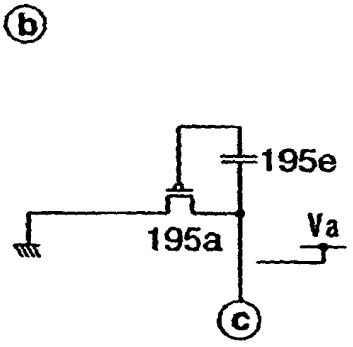


Fig. 30D1

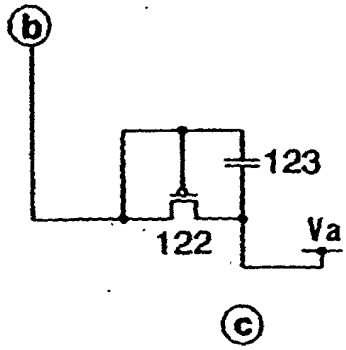


Fig. 30D2

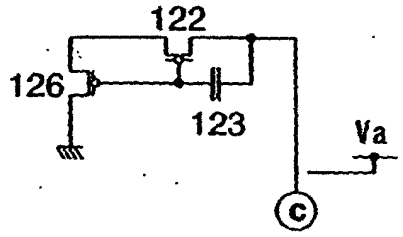
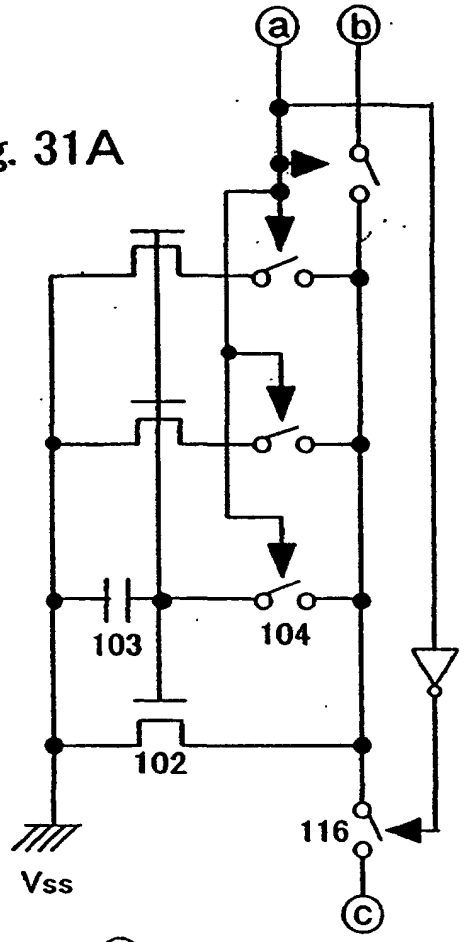


Fig. 31A



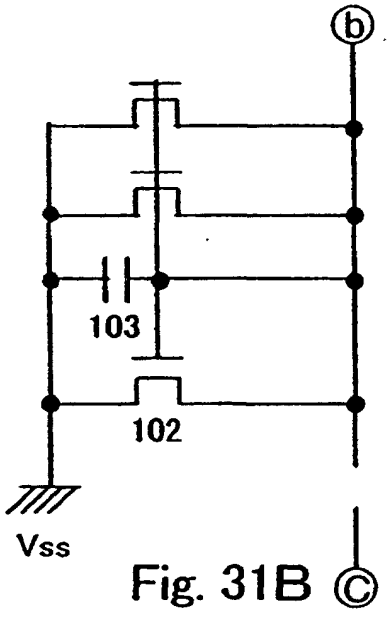


Fig. 31B

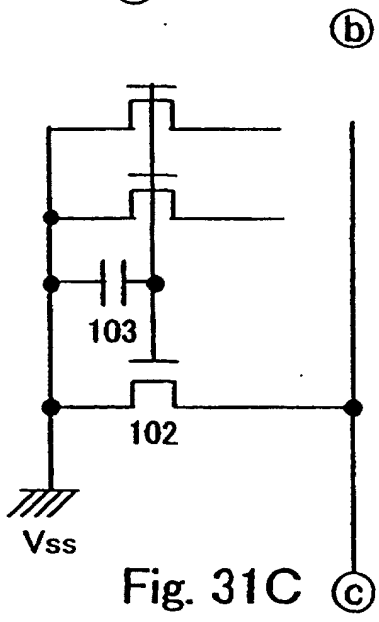


Fig. 31C

Fig. 32

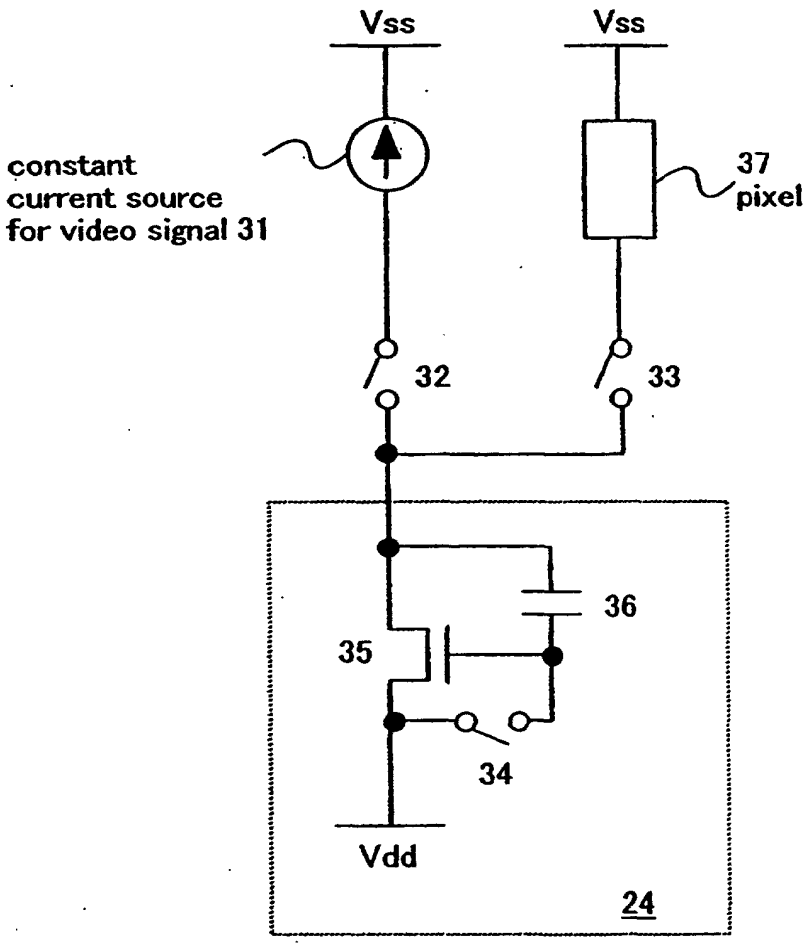

Vss
Vss
constant
current source
for video signal 31
37
pixel
32
33
36
35
34
Vdd
24

Fig. 33

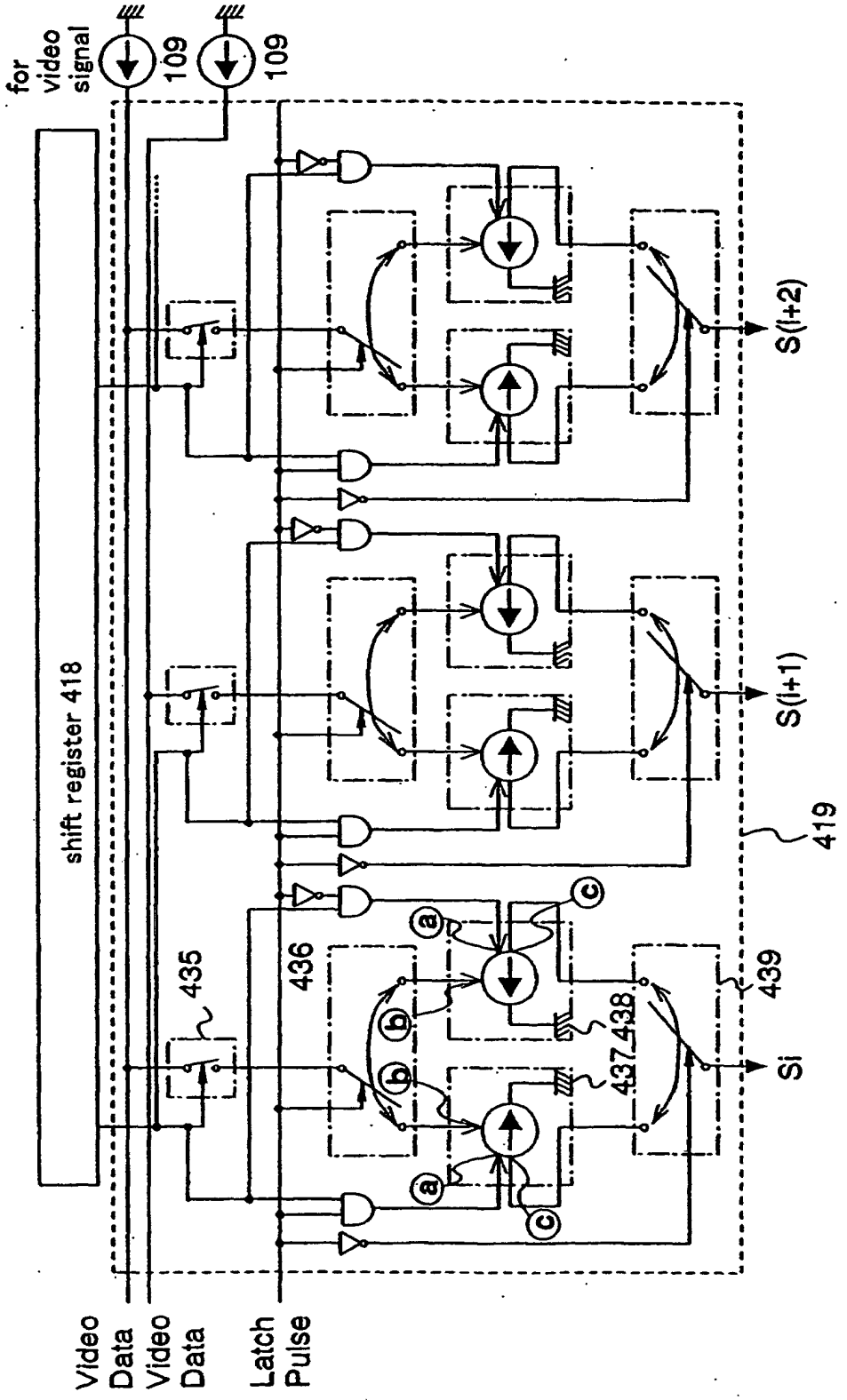

for video signal
109
109
shift register 418
S(i+2)
S(i+1)
419
435
436
439
438
437
Si
a
b
c
Video Data
Video Data
Latch Pulse

Fig. 34

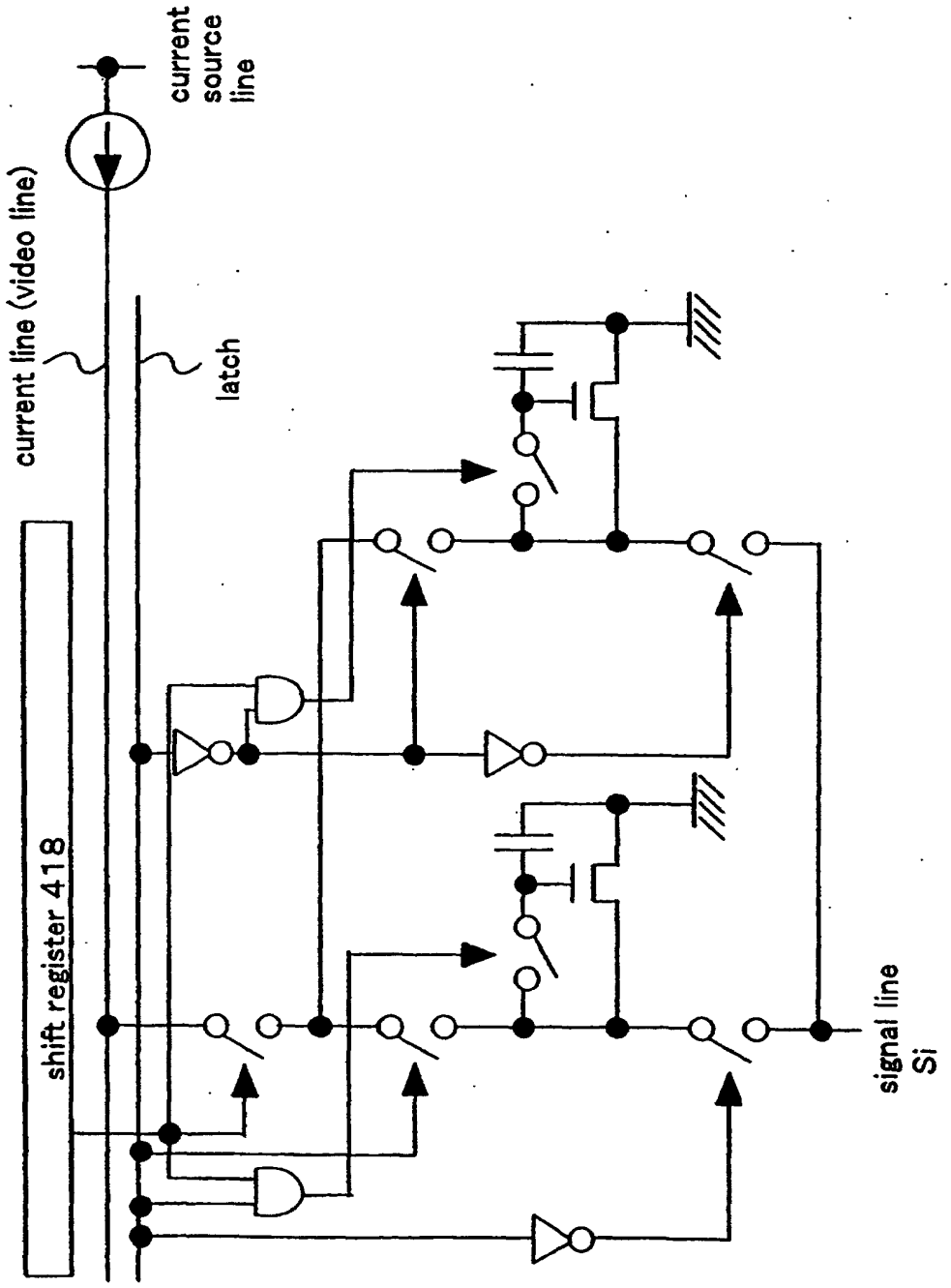

current source line
current line (video line)
latch
shift register 418
signal line Si

Fig.35

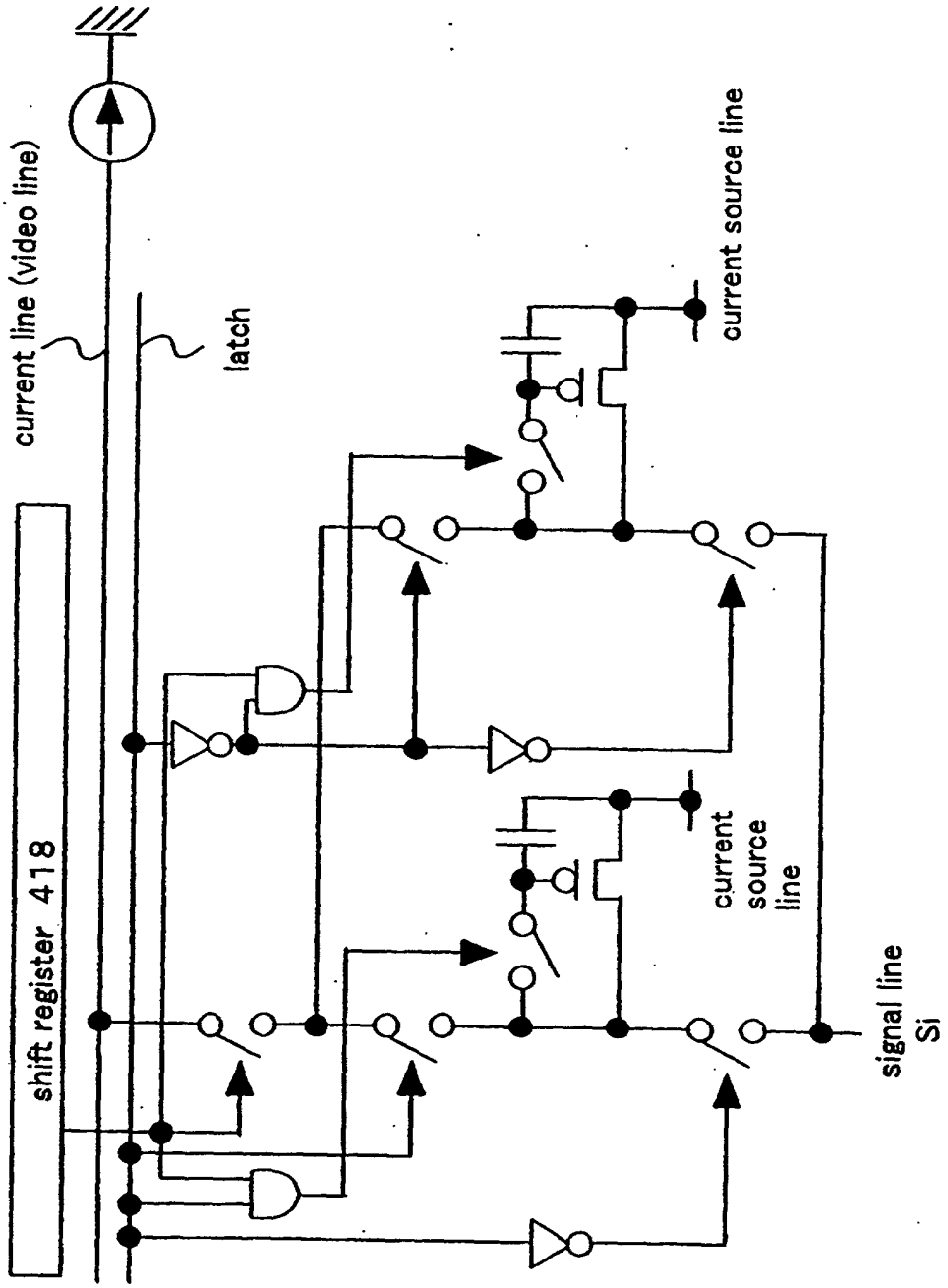

current line (video line)
latch
current source line
shift register 418
current source line
signal line Si

Fig. 36

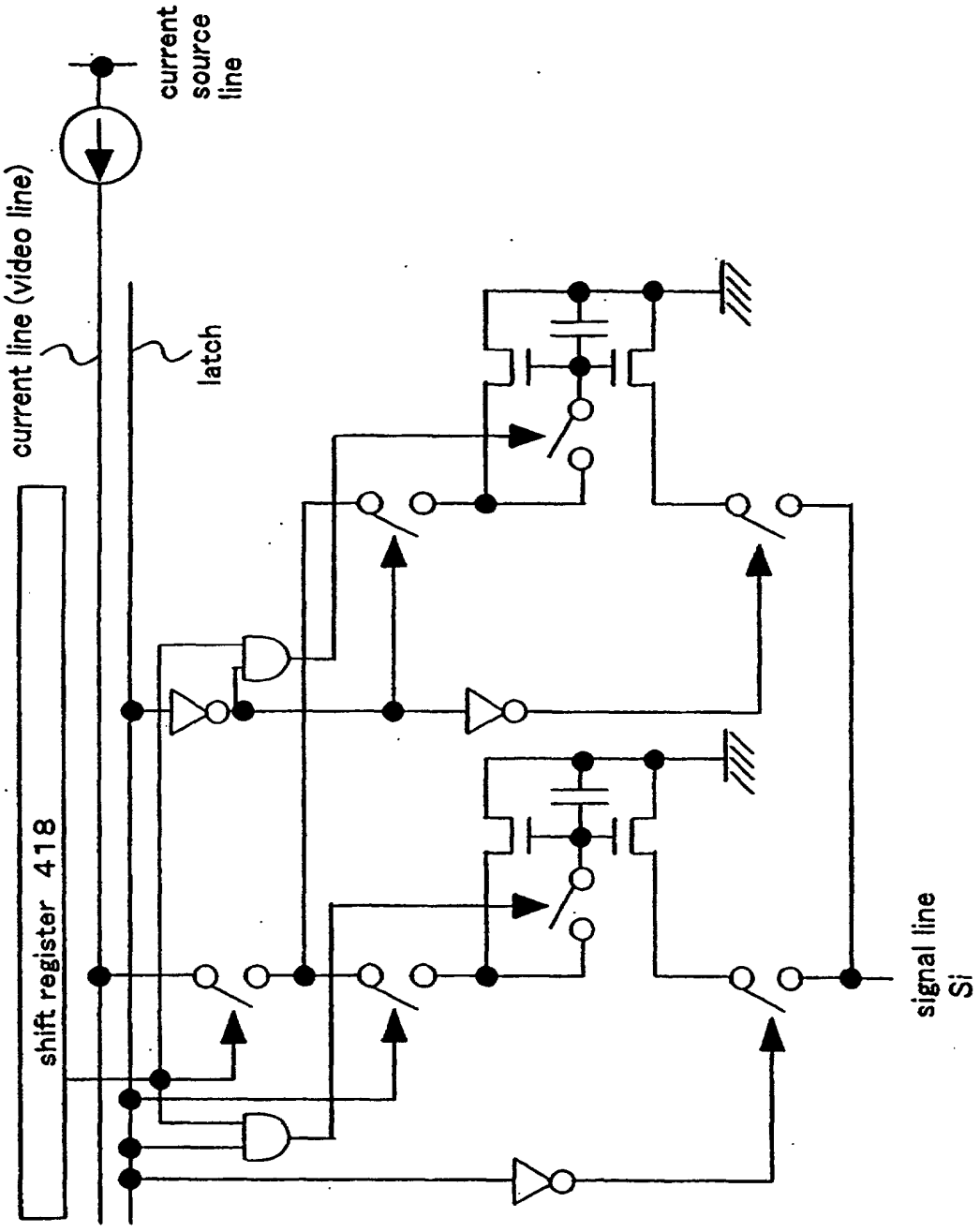

current source line
current line (video line)
latch
shift register 418
signal line Si

Fig. 37A

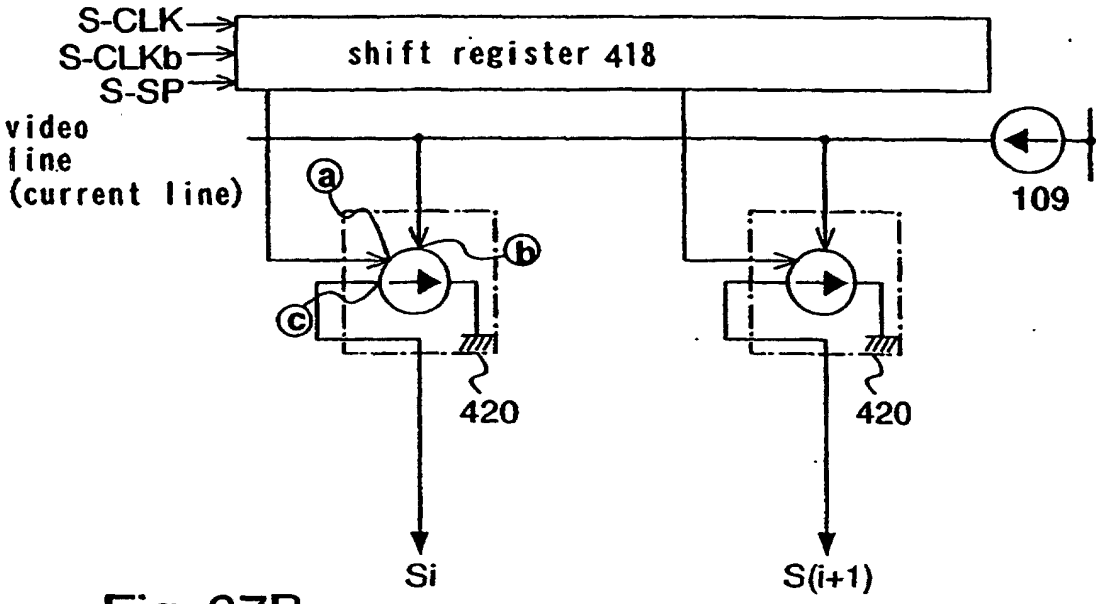


Fig. 37B

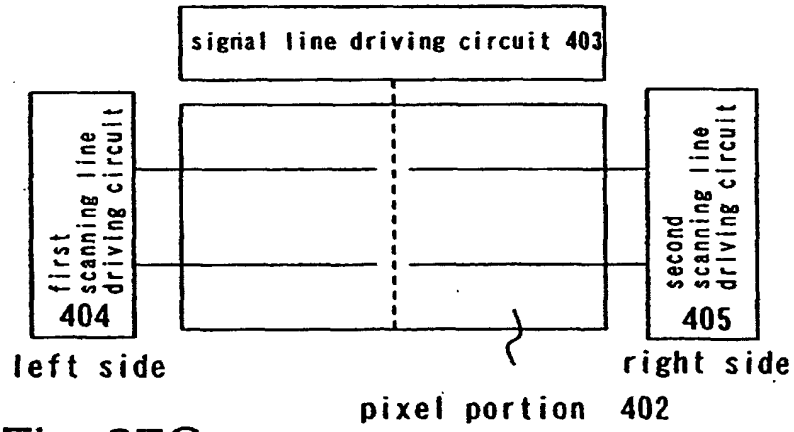


Fig. 37C

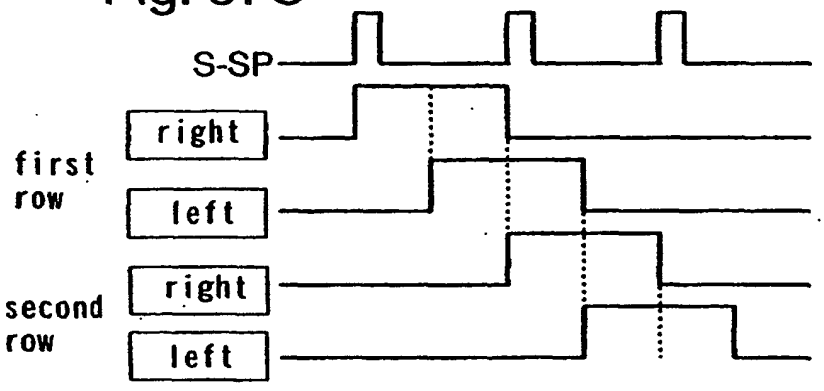


Fig. 38

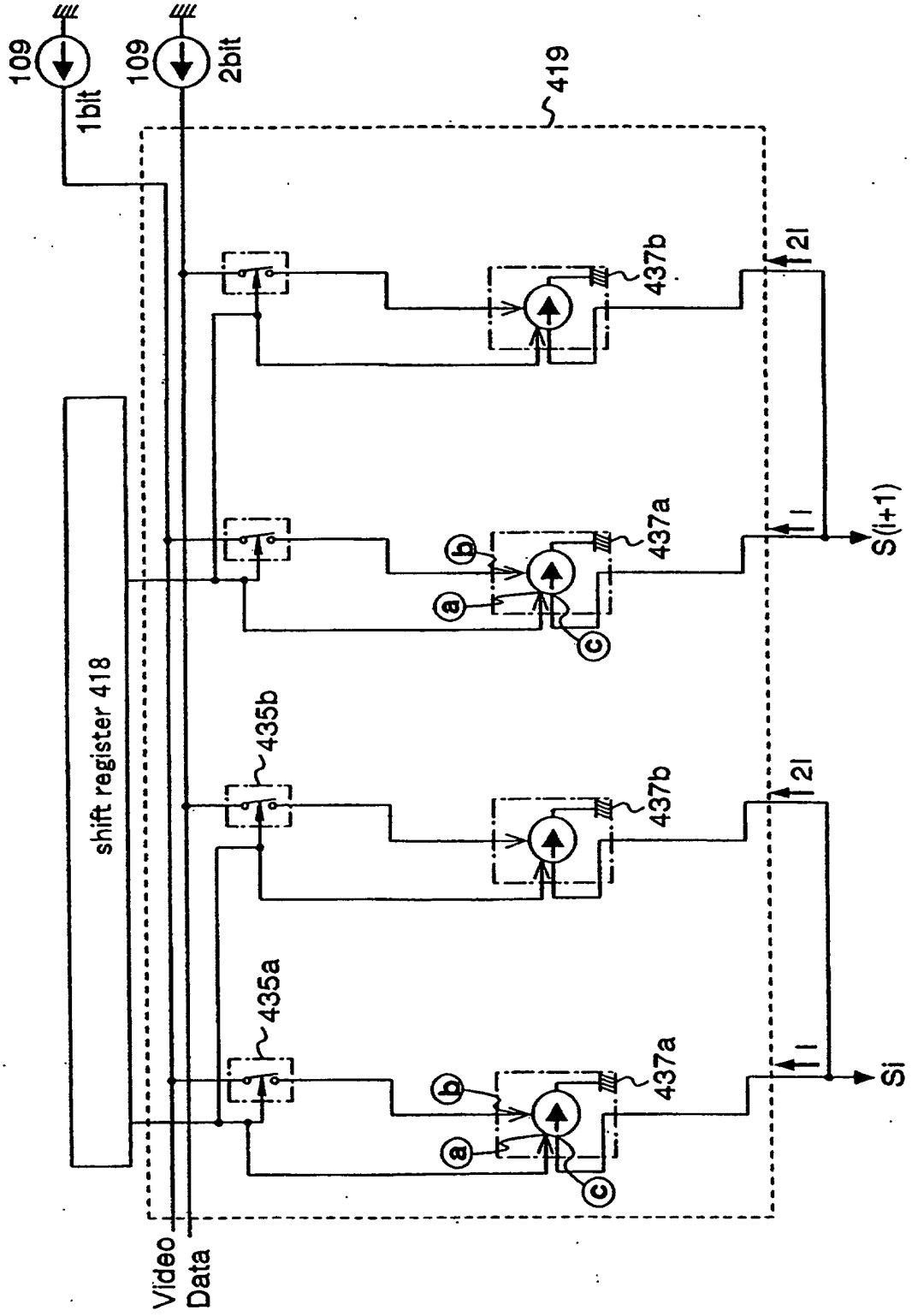

109
1bit
109
2bit
419
437b
2I
437a
I
S(i+1)
shift register 418
435b
437b
2I
435a
437a
I
Si
Video Data

Fig. 39

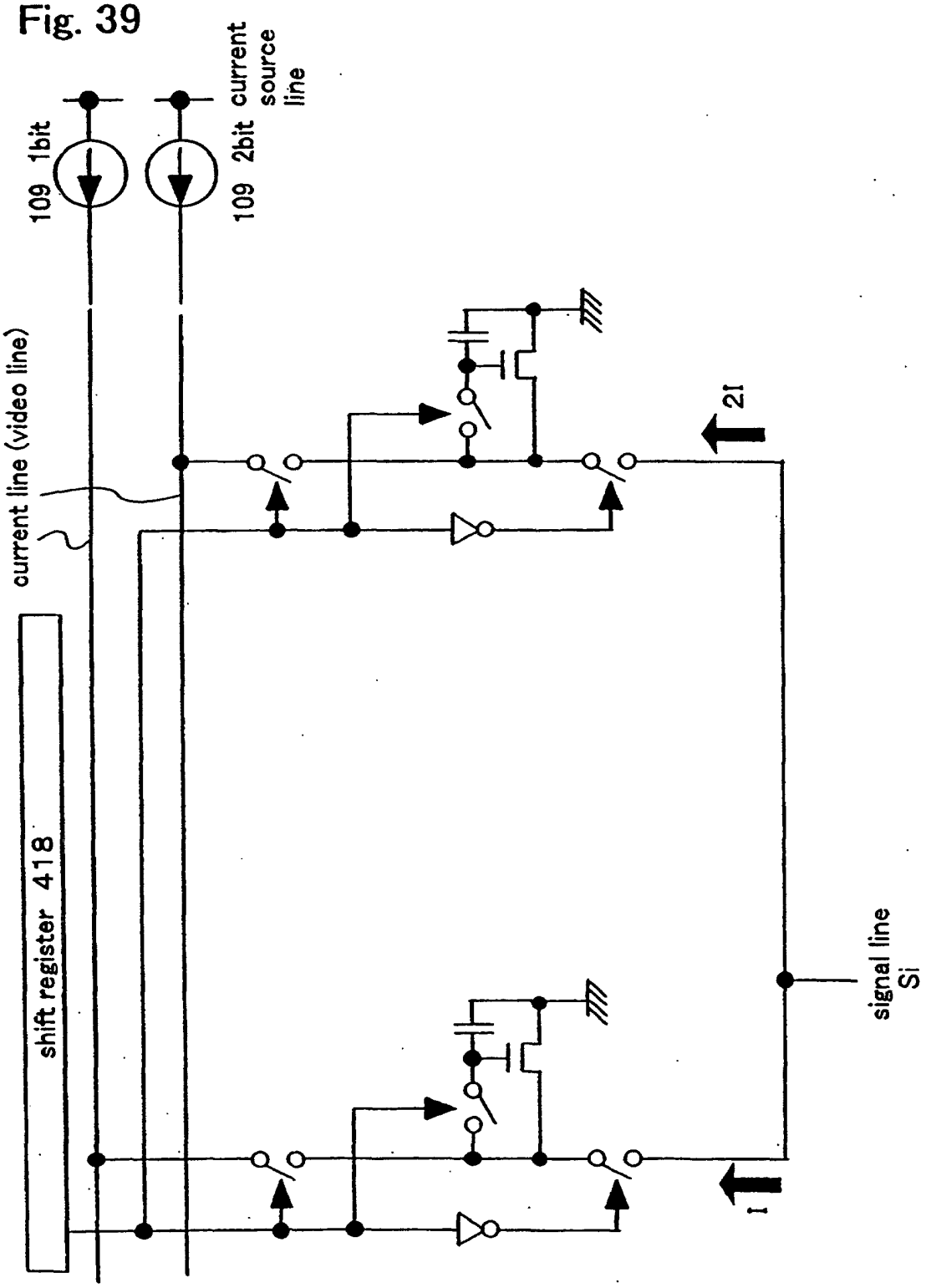

109 1bit
109 2bit
current source line
current line (video line)
shift register 418
2I
I
signal line Si

Fig. 40

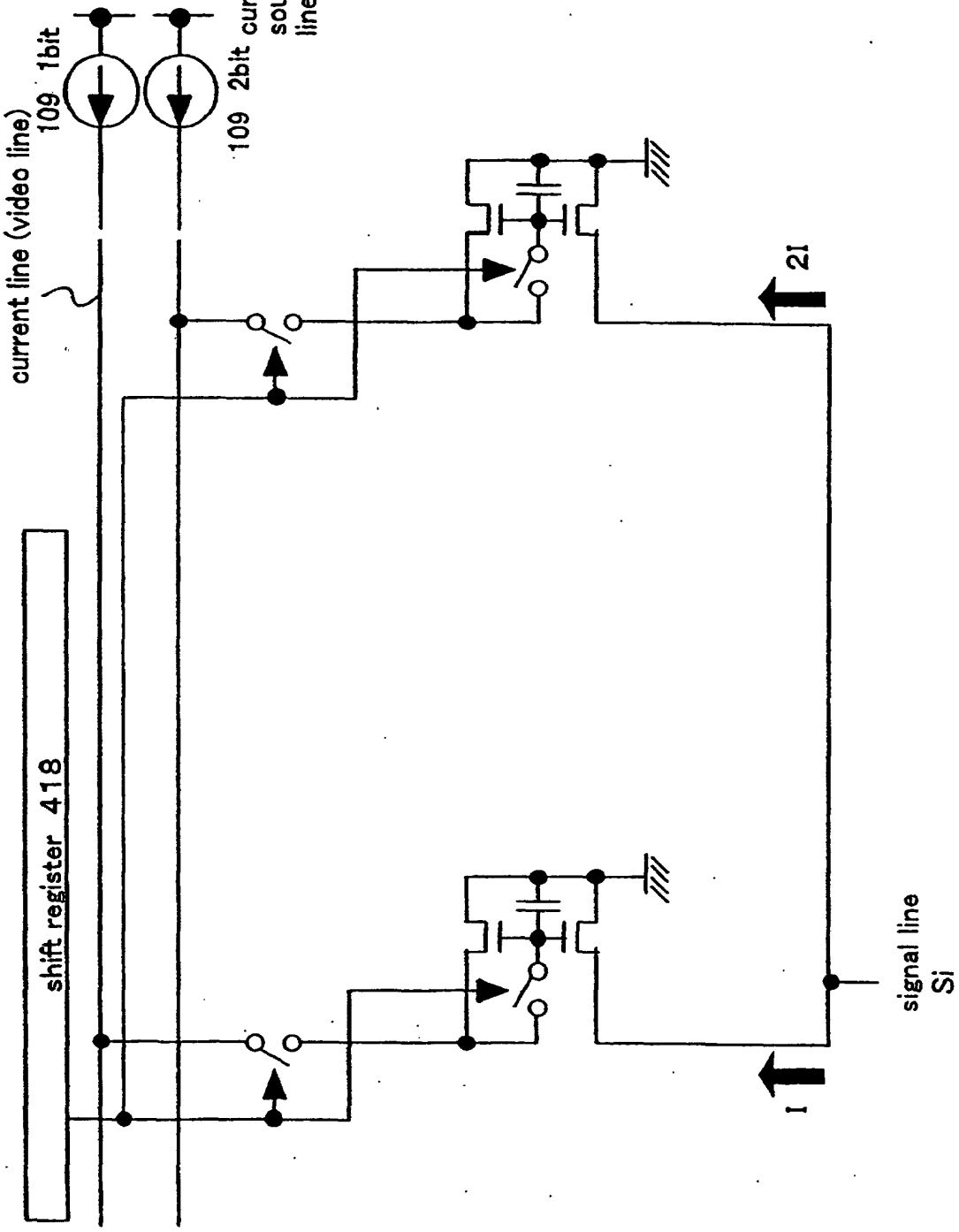

current line (video line)
109 1bit
109 2bit current source line
shift register 418
2I
I
signal line
Si

Fig. 41

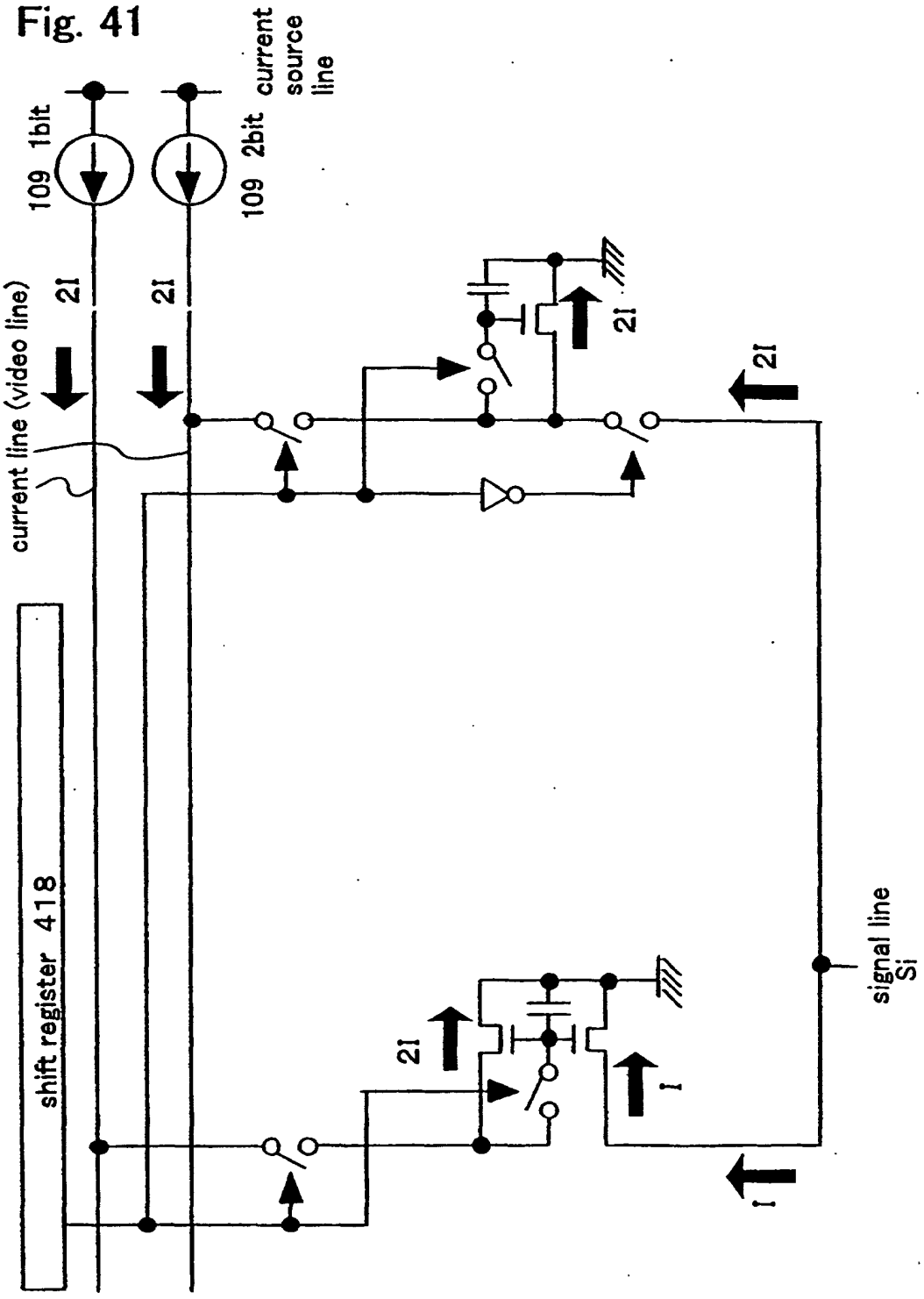

109 1bit
109 2bit
current source line
current line (video line)
21
21
21
21
21
I
I
shift register 418
signal line
Si

Fig. 42

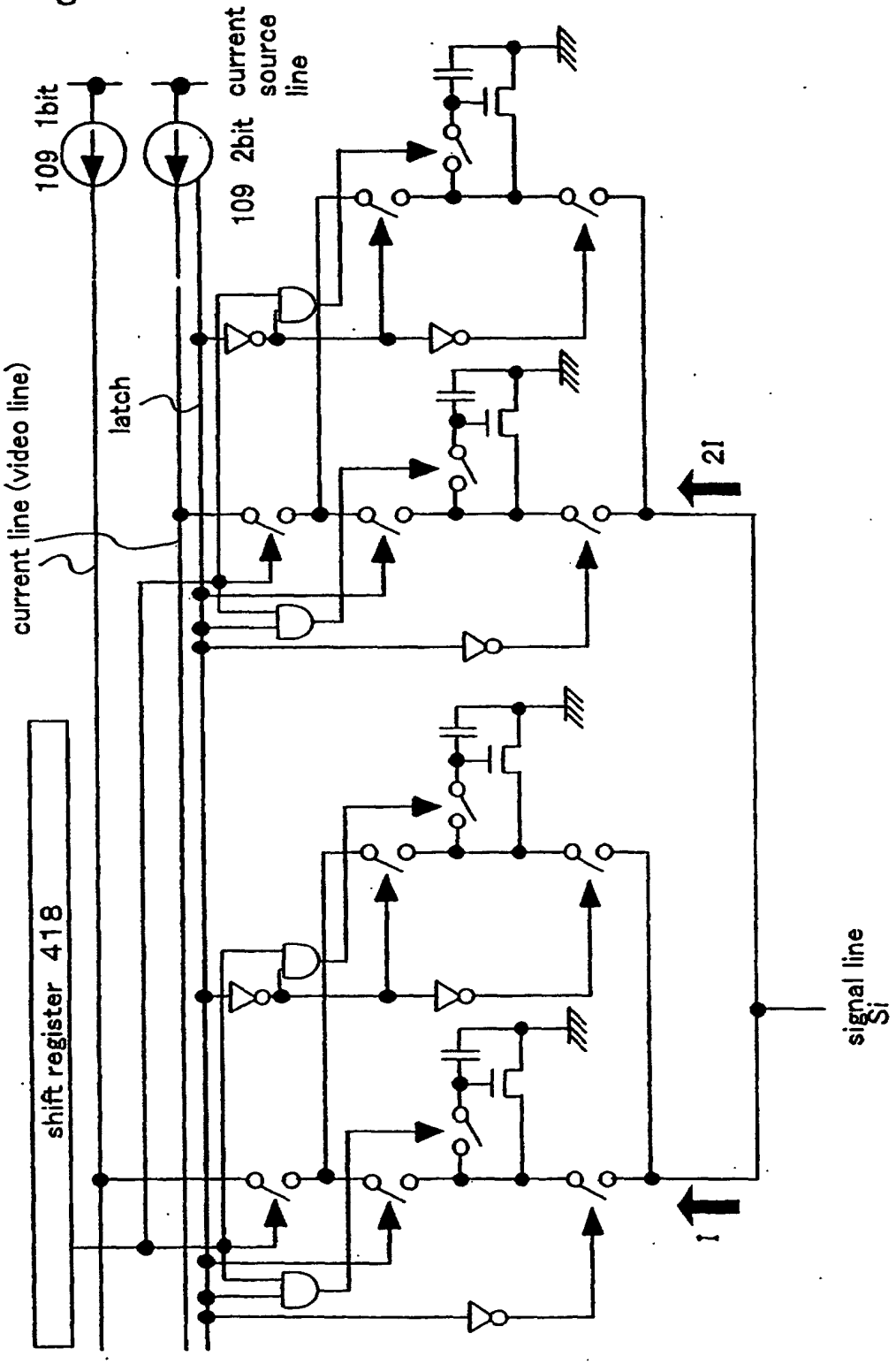

109 1bit current source line
109 2bit
latch
current line (video line)
shift register 418
21
1
signal line Si

Fig. 43

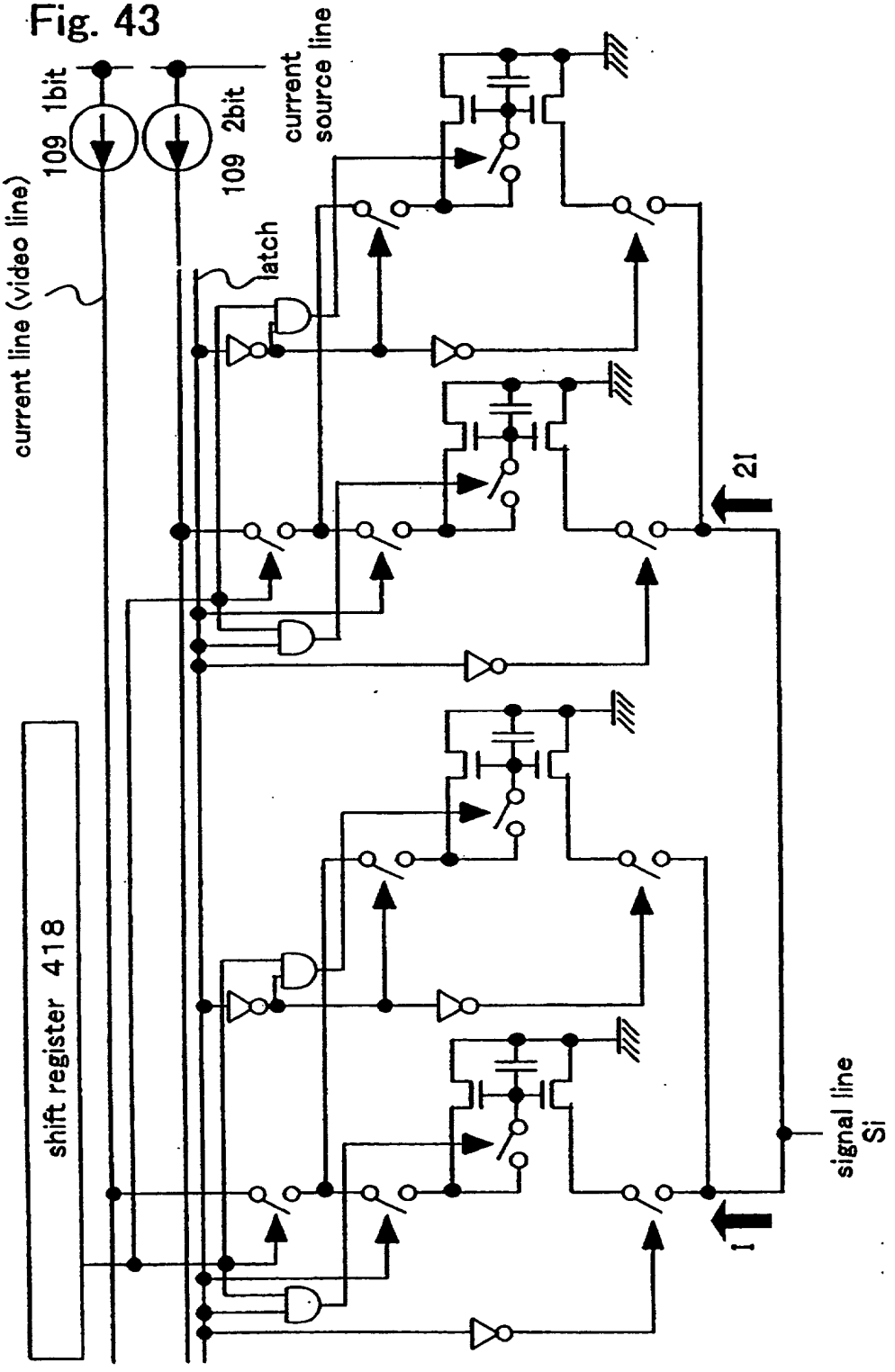

current line (video line)
109 1bit
109 2bit
current source line
latch
shift register 418
21
signal line Si

Fig. 44

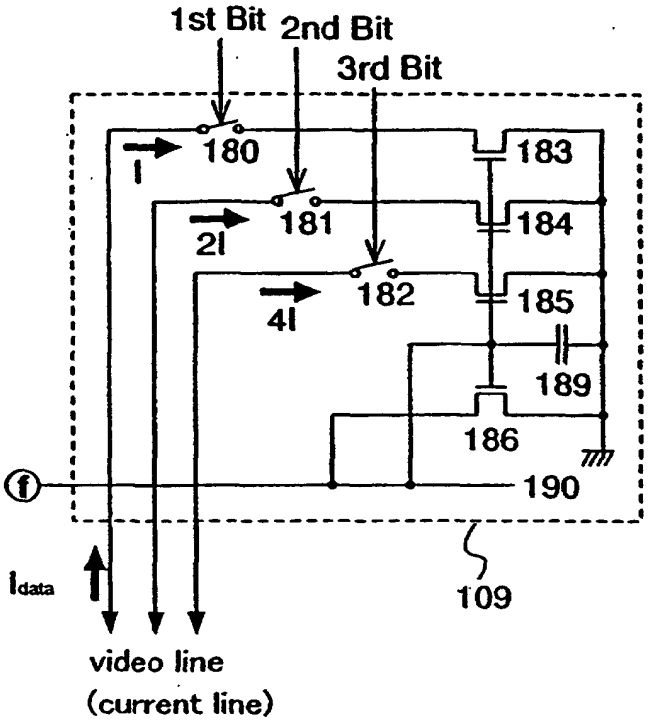

1st Bit
2nd Bit
3rd Bit
180
181
182
183
184
185
186
189
190
I
2I
4I
Idata
109
video line
(current line)

Fig. 45

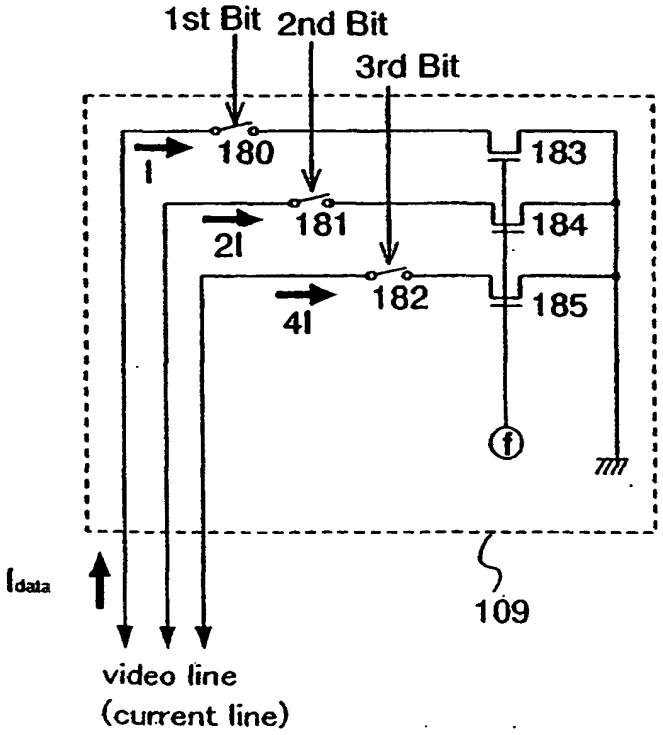

1st Bit
2nd Bit
3rd Bit
180
181
182
183
184
185
I
2I
4I
Idata
109
video line
(current line)

Fig. 46

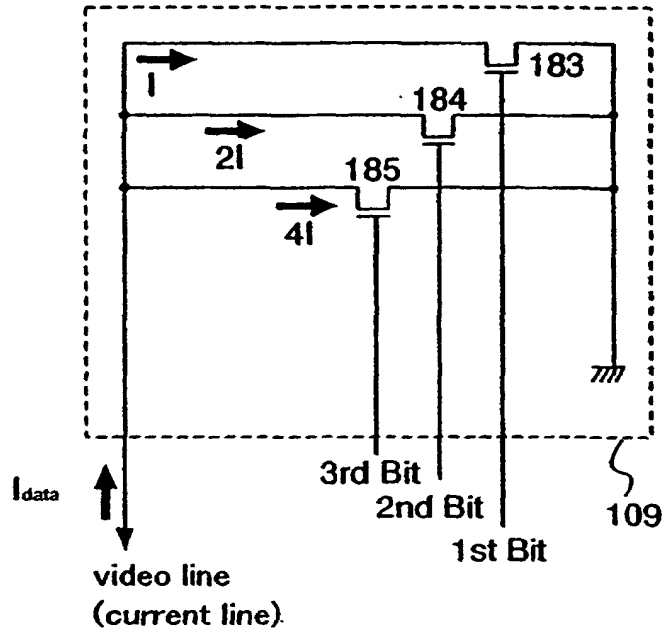

I
2I
4I
183
184
185
3rd Bit
2nd Bit
1st Bit
109
I_{data}
video line
(current line)

Fig. 47

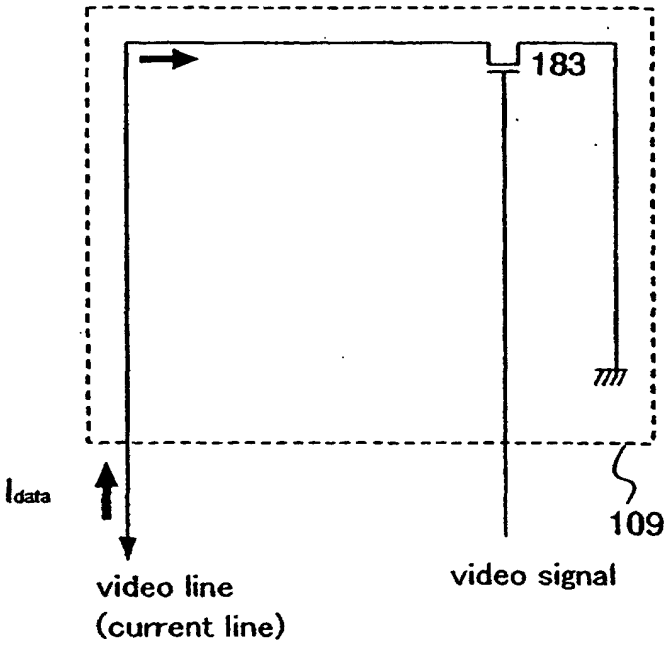

183
109
I_{data}
video line
(current line)
video signal

Fig. 48

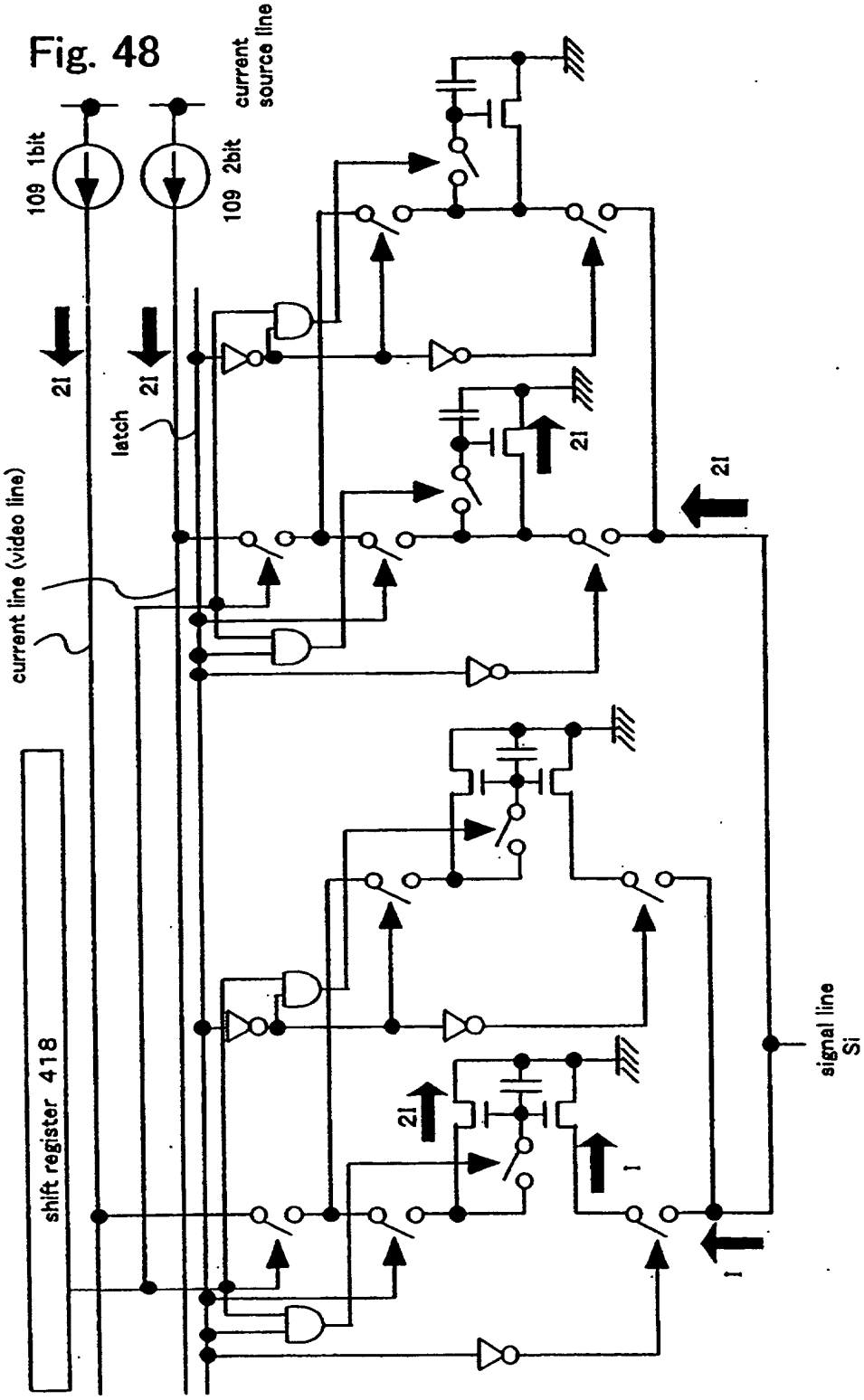

current source line
109 1bit
109 2bit
2I
2I
latch
2I
2I
current line (video line)
shift register 418
signal line
Si
2I
I
I

Fig. 49

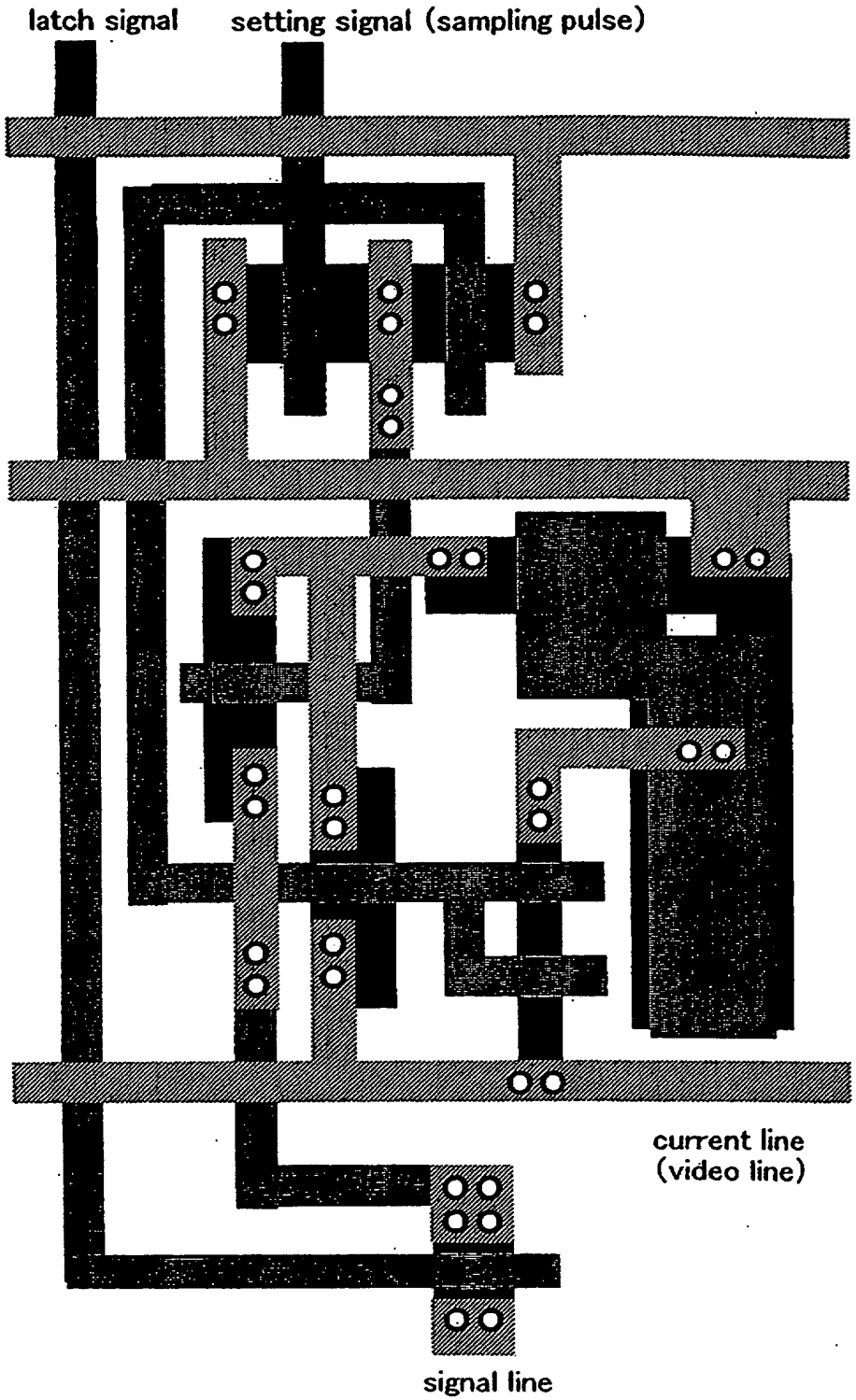
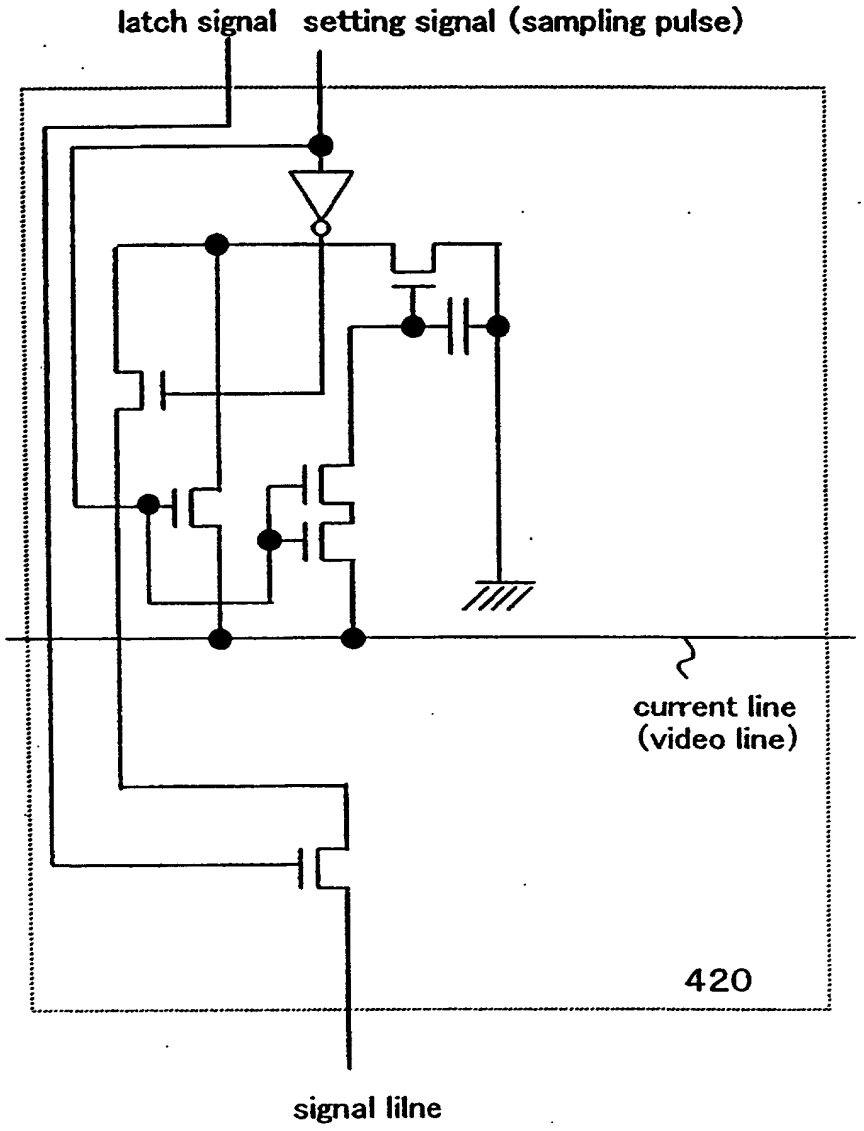

latch signal
setting signal (sampling pulse)
current line
(video line)
signal line

Fig. 50


latch signal
setting signal (sampling pulse)
current line
(video line)
420
signal lilne

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP02/11355

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G09G3/30, G09G3/20, G05F1/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G09G3/30, G09G3/20, G05F1/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-2003
Kokai Jitsuyo Shinan Koho 1971-2003 Jitsuyo Shinan Toroku Koho 1996-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
JICST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2000-81920 A (Canon Inc.), 21 March, 2000 (21.03.00), Par. Nos. [0005] to [0018]; Figs. 1, 5 & US 6222357 B1	1-3,5-15
Y	Microfilm of the specification and drawings annexed to the request of Japanese Utility Model Application No. 10861/1986 (Laid-open No. 122488/1987) (Sony Corp.), 04 August, 1987 (04.08.87), Description, pages 6 to 9; Figs. 1 to 4 (Family: none)	1-4,7,12-15
Y	JP 11-282419 A (NEC Corp.), 15 October, 1999 (15.10.99), Par. Nos. [0038] to [0083]; Figs. 1 to 14 & US 6091203 A & KR 99078420 A	1-3,5-15

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 February, 2003 (10.02.03)	25 February, 2003 (25.02.03)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP02/11355

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 6-118913 A (Casio Computer Co., Ltd.), 28 April, 1994 (28.04.94), Par. Nos. [0002] to [0003], [0016] to [0053]; Figs. 1 to 6 (Family: none)	1-15
Y	JP 2001-290469 A (NEC Corp.), 19 October, 2001 (19.10.01), Par. Nos. [0024] to [0034]; Figs. 1 to 2 (Family: none)	1-15
Y	JP 8-95522 A (Toppan Printing Co., Ltd.), 12 April, 1996 (12.04.96), Par. Nos. [0007] to [0025]; Figs. 1 to 5 (Family: none)	12
Y	JP 11-231834 A (Pioneer Electronic Corp.), 27 August, 1999 (27.08.99), Par. Nos. [0033] to [0038]; Figs. 4 to 6 & US 6473064 B1	1-15

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